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DECEMBER 2005
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The Magazine for Developers of Open Communication, Industrial, and Rugged Systems

2006 Buyer's Guide

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DECEMBER 2005

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The Magazine for Developers of Open Communication, Industrial, and Rugged Systems

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COVER

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FCI's AirMax VS coplanar connector allows for the easy insertion of add-in boards for system upgrades, memory expansion, and test.
(Row 2 left to right)
F9 Systems, Inc. Tx/Rx SignalBlade and Tx/Rx BenchBlade facilitate detailed signal integrity analysis of HM-zd based backplanes and logic cards. F9 Systems offers turnkey hardware verification test solutions for signal integrity, power, and thermal analysis.
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Maximizing backplane switching performance of AdvancedTCA systems
By Matthias Lim, Enigma Semiconductor and Sorin Vasile, Elma Trenew Electronic

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EDITOR'S FOREWORD

Happy Birthday, CompactPCI – You're stronger, faster, and better

By Joe Pavlat

CompactPCI & AdvancedTCA

November, 2005 marked the tenth anniversary of the ratification of the original CompactPCI specification. A great deal has happened in those 10 years, including technology evolution and broad market acceptance. Many of those developments paved the way for sophisticated next generation technologies like AdvancedTCA and the Advanced Mezzanine Card.

Simple beginnings

The original idea was simple: leverage ubiquitous PCI silicon available from a growing base of silicon and CPU providers to create a rugged, flexible, high performance open platform for industrial computing. At least two of the original developing companies, including mine, embraced the concept as a replacement for the aging STD bus. After a couple of passes at a new mechanical form factor, the group embraced the available and proven IEEE 1101 mechanics popularized by the VMEbus a decade earlier. The high density 2 mm connector was an IEC standard available from a variety of manufacturers. Providing up to 615 pins on a 6U card, this connector enabled a host of interconnects beyond the basic data bus, enabling rear panel transition modules and secondary buses like H.110 for telephony. The ability to easily build these connectors with multiple length pins led the way to the first viable hot swap standard. And that was just the beginning. CompactPCI has evolved over the years adding significant industry "first" capabilities, including:

- First hot swap capability (PICMG 2.1)
- First support for H.110 telephony bus (PICMG 2.5)
- First open System Management specification (PICMG 2.9)
- First switched fabric backplane (PICMG 2.16 using Ethernet), followed by Starfabric (PICMG 2.17), and RapidIO (PICMG 2.18)

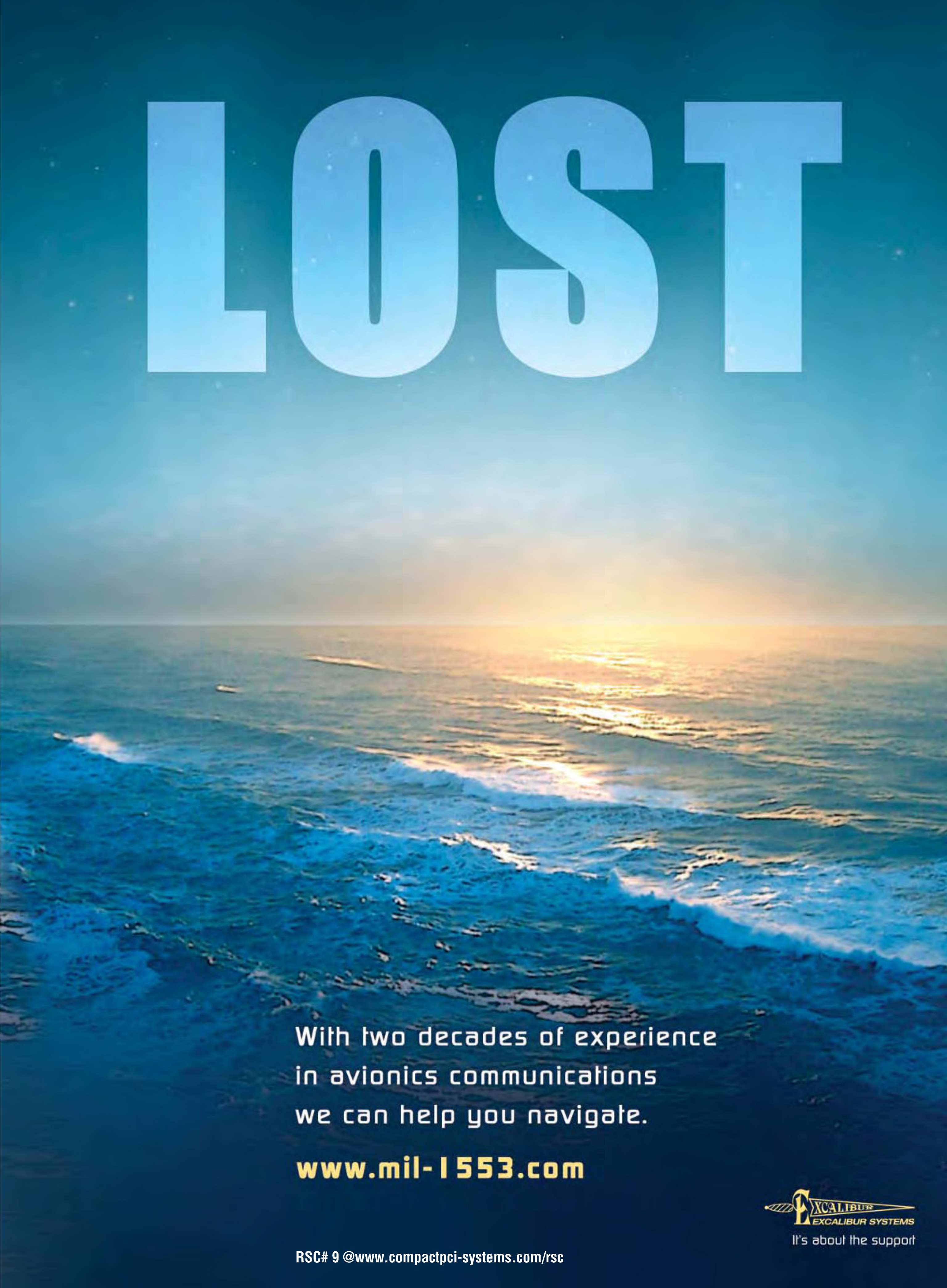
The industry's first switched fabric platform

PICMG 2.16, usually known as CompactPCI 2.16, was a significant technology advance, adding standard 10/100/1000 Ethernet to the backplane in a redundant, dual star configuration. The parallel PCI bus became optional. Maximum data throughput shot up to over 40 gigabits per second (Gbps) and CompactPCI remained the fastest, highest throughput open standard available. Reliability improved with the fabric backplane, as the failure of a single board did not usually fail the entire system, which was a weakness of earlier buses like VME and parallel PCI.

The toughest robot race in the world – powered by CompactPCI

In an effort to encourage the development of autonomous vehicle navigation for future military applications, the Defense Advanced Research Projects Agency (DARPA) has, for the last several years, sponsored a brutal road race across 150 miles of rough terrain, desert, ravines, tunnels, hills, and obstacles. The vehicles must operate completely autonomously – no remote control is allowed – and complete the 150 mile course in less than 10 hours. No vehicle completed the race until this year, when five vehicles crossed the finish line in time. The winning team took home the $2 million prize. The top three finishing vehicles – one from Stanford University (Figure 1, courtesy of DARPA) and two from

Figure 1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Carnegie Mellon – were all powered by CompactPCI 2.16 systems that integrated complex vision and sensor systems, artificial intelligence, and vehicle control. Move over, VME.

The pioneering groundwork of CompactPCI 2.16 has led to a broad acceptance of managed, redundant, switched serial interconnect technology and to the development of newer, faster, and more powerful platforms based on the technology, including AdvancedTCA and the Advanced Mezzanine Card. But these newer fabrics are now being integrated into CompactPCI, making the platform ever better, faster, and more robust.

Getting faster yet

Of note is the recently ratified CompactPCI Express Specification, which is based on the PCI Express standard. Developed by Intel and backed by the enormous volumes of the desktop PC market, PCI Express will likely be as ubiquitous and popular as the original PCI bus. Being a switched serial interconnect, it is more robust and scalable. In addition, PCI Express is capable of error correction and full redundancy. And it is fast. Very fast. While the original 32-bit PCI bus was fast for its day, offering 132 megabytes per second (MBps) data transfer rates when competing technologies provided a fraction of that, PCI Express is capable of moving a blazing 8000 MBps, in its x16 configuration. CompactPCI Express promises to be a major platform for a variety of I/O intensive applications. Among them are vision and imaging systems for everything from automated inspection to homeland security and military applications (see Lee Brown's article on using CompactPCI and CompactPCI Express for advanced Helmet Mounted Displays in this issue, page 30).

Along the way, CompactPCI has expanded well beyond its simple origins as an industrial computer bus to be a leading technology for advanced communications, media gateways, telephony, test and measurement, and military and avionics platforms. With the recent announcement of radiation-hardened systems, it's even moving into space.

CompactPCI has indeed come a long way, and if the last 10 years are any predictor of the future, continued innovation will occur. This is not just a testimony to the sound fundamentals of the technology, but also to the engineers and marketing professionals in the 450 PICMG member companies. It is their experience, knowledge, and willingness to work collaboratively to develop strong open standards that has helped PICMG specifications like CompactPCI remain fresh and successful. The last 10 years have been a lot of fun, and I'm looking forward to the next 10 with great enthusiasm.

Joe Pavlat
Editorial Director

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Winning at the slots: Strategies for complying with PICMG ECN Shelf Thermal Requirements 5.4.2

By Jason Leboeuf

The PICMG ECN specification for AdvancedTCA requires shelf manufacturers to provide an abundance of airflow characterization data for board design use. Although the specification clearly states these requirements, it does not detail the methods to be used in obtaining the data. Jason provides elaboration on the pertinent sections of the standard as well as examples of test methods used to analytically and empirically fulfill the PICMG thermal requirements.

Introduction

AdvancedTCA's role as an open industry standard provides significant flexibility to both the manufacturer and consumer of the final system level product. The AdvancedTCA specification provides a versatile solution that allows for a variety of opportunities and functions for shelf and board makers. Manufacturers can then pass this same versatility on to end users, allowing them to satisfy a multitude of needs solely through the AdvancedTCA technology base.

On the other hand, when examining additional aspects of the AdvancedTCA concept, the challenges faced in obtaining this versatility quickly become evident. This rings especially true when looking at the area of thermal management. As is the case in almost all of the electronics industries, managing the ever-increasing heat load of faster and more capable components has become extremely challenging. To manage this against the criteria of a single application from a single manufacturer is an effort in itself, and becomes even more challenging against the metrics of an open industry standard created for countless applications from countless manufacturers. This is why the documentation and interpretation of section 5.4 of the PICMG ECN standard, *Shelf Thermal Requirements*, has become a critical topic.

Due to the previously emphasized wide-ranging audience for the PICMG ECN standard, section 5.4's thermal guidelines for shelf manufacturers are very broad in their requirements. This is an attempt to encompass all shapes, sizes, and most importantly airflow regimes of all the shelf level products that PICMG members may introduce into the AdvancedTCA marketplace. The goal behind this catering to all shelf manufacturers is to supply the corresponding PICMG card manufacturers with an accurate portrayal of each shelf's airflow characteristics, features which can then be used to design and test each new card product.

What follows is a section-by-section breakdown and discussion of how to comply with and obtain the necessary data to fulfill section 5.4.2, *Slot Cooling Capability.*

For purposes of this discussion, the Equipment Under Test (EUT) will be a 22.75-inch (13U) chassis with 14 vertically oriented boards. The air delivery system will be comprised of four horizontal blowers, all located above the boards and exhausting directly out the rear of the chassis. To add realism to the test matrix the blowers will have two operating speeds: nominal (50 percent) and high (100 percent). In addition to the dual fan speeds, the system will be tested with two sets of test boards; 14 boards with no impedance (0 percent blockage) and 14 boards fitted with a thin *lip* near the card's leading edge. The lip will extend the length of the card, front to rear, and the height will be 70 percent of the board pitch (70 percent blockage). Although this impedance is not a true volumetric resistance, it will deter airflow and therefore aid in the cooling of the populated slots. Figure 1 is an example of a test card, or *slot blockers,* outfitted with a number of air velocity sensors.

5.4.2.1: Slot impedance curve

The standard states that "the shelf manufacturer shall determine pressure drop versus volumetric airflow rate curve or the slot impedance curve for each empty front board slot within the shelf over the intended operating range" and shall provide one of the following:

- A single curve for the shelf that accounts for worst-case slot airflow if all slots have impedance curves at a given pressure differing from each other within ±10 percent.
- The slot impedance curve for outlying slots in addition to the (otherwise worst-case) slot airflow.
- The slot impedance curve for each slot.
- The slot impedance curve(s) may be determined by analysis, simulation, or empirical testing.

Interpretation

At first examination, the standard's request for manufacturers to obtain pressure drop seems a bit confusing, considering that the pressure inside a single slot during any system operation is not represented by an entire curve but simply by a single pressure reading. In order for the static pressure readings inside a system to compose, for example, a slot impedance curve, a volume of air that is increasing or decreasing in flow rate must be present. One instance would be an impedance curve taken on a test card utilizing an airflow test chamber where the static pressure can be monitored and the flow rate can be adjusted from zero to some upper

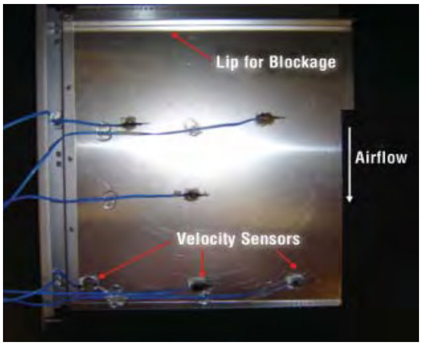

Figure 1

limit such as 100 cubic feet per minute (cfm). As the conditions just described don't exist inside a system running at a set fan speed, the best that can be provided is the location of the operating point on the test card's impedance curve, for each slot, at each fan speed. After examining multiple possible solutions, IQS devised the following test method by utilizing empirically derived data as well as a number of calculations, both of which the standard recognizes as acceptable means of determining the results.

Test method

The test data necessary for the method came from two different tests. The first was *air catch* data, which can also be defined as the total volumetric flow rate of a system. This consists of a single value measured in either cfm or cubic meters per minute (cmm), and is usually obtained by attaching the system exhaust directly to the inlet of a wind tunnel or airflow test chamber, which then measures the total output of the system. We decided to use this as the foundation of the test method because we preferred to base the necessary calculations on empirical data whenever possible. Therefore, as Table 1 shows, the air catch data for four different cases was used.

A different air catch value was necessary for each of the four scenarios because changing either the fan speed or the amount of blockage on each card can drastically affect the air movers' ability to pass air through the chassis. For each case the air catch value was broken down into an average volumetric flow rate for each slot to be used later in the calculations.

Along with the air catch data, velocity profile data was also necessary. We obtained velocity profile data by using a test card, for both blockage values, outfitted with three velocity probes on the leading edge of the card. Inserting the cards one at a time into each slot of the chassis at the different air mover speeds (low and high) captured the velocity data at each of the probe locations. Once collected, the data was formatted and an average inlet velocity for each card was then calculated by averaging the data from all three probes. For each test case the average inlet velocities for each slot were then averaged again to obtain the average inlet velocity for the chassis. Once we obtained this value we used it to calculate the amount that each card's average inlet velocity deviated from the average inlet velocity of all the slots in the chassis. Applying this deviation value to the average volumetric flow rate previously calculated enabled us to calculate each slot's flow rate. The flow rate data was then combined with the impedance curve for the test card by plotting both pieces of data on the same x/y plane. The resultant data for all 14 slots, with 70 percent blockage under

		Blower Speed	
		Low	High
Blockage	0%	X	X
	70%	X	X

Table 1

a high fan speed condition is shown in Table 2. Figure 2 also shows the first four slots plotted against the slot impedance curve.

Although it is not displayed in Figure 2, this method allows all slots in the chassis to be plotted on the same graph for each test condition. Each vertical line represents a different slot and the intersection of each vertical line with the test card's impedance curve represents the static pressure measurement (operating point) of the slot, or the *slot impedance.*

This approach makes a number of assumptions by using the average flow rate and average inlet velocity. However, employing empirical data provides the validity needed for future testing by card manufacturers. One benefit to both shelf and board manufacturers utilizing this test method is that the calculations help to very quickly point out the shelf's strengths and weaknesses in regards to the possible card locations. It becomes clear where the board manufacturer should use extra caution in locating products, as well as where the shelf manufacturer can improve on the cooling scheme.

5.4.2.2: Slot fan flow curve

The second major part of the PICMG standard requiring interpretation as an established test method is 5.4.2.2, Slot Fan Flow Curve. This section of the standard states:

"The shelf manufacturer shall determine the pressure drop versus volumetric airflow rate curve for the fan behavior of the slot fan flow curve for each empty front board slot within the shelf over the intended operating rage. The slot fan flow curve shall capture the various operating modes supported by the shelf if they apply, such as low-medium-high speed or fan failure."

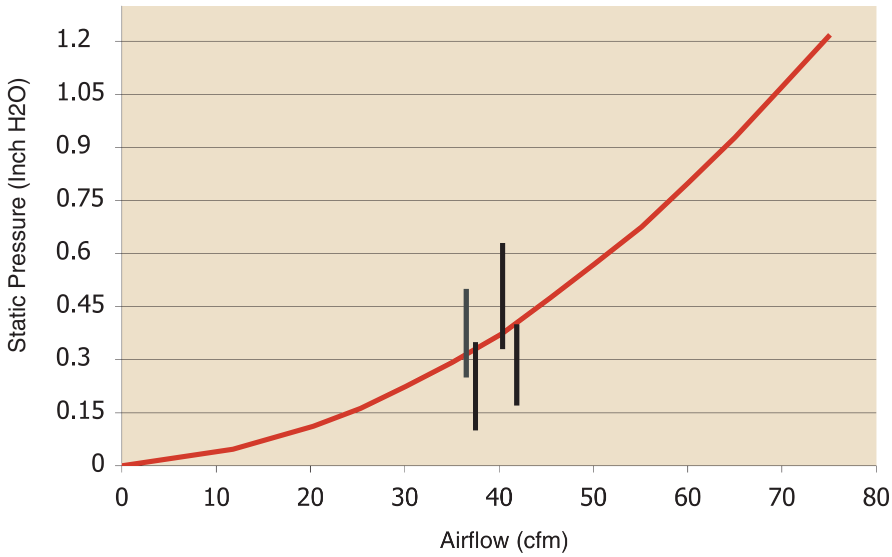

Figure 2

The slot fan flow curve may be determined through analysis, simulation, or empirical testing.

Interpretation

Again the standard is requesting data that upon first look seems to be somewhat intimidating to capture. The term *slot fan flow curve* can also be defined as a fan performance curve in relation to each individual slot in the chassis. To further simplify, the standard is requesting data showing how the volumetric flow rate of each slot is affected by a blockage, typically ranging from wide open to fully impeded. This information, as in section 5.4.2.1, is not simply collected through a typical laboratory test due to it being physically impossible to take pressure and flow rate measurements for a single slot inside an operating chassis. However, this problem can be solved by obtaining a small amount of empirical data and utilizing a simple fan law. The result will be a representative curve for each slot at each of the system's fan speeds and as for a fan failure scenario, one that will account for one less fan with the remaining fans operating at high speed. The following test method provides

Slot	Flow Rate (cfm)
1	36.5
2	37.5
3	40.4
4	41.9
5	41.5
6	42.2
7	40.0
8	40.7
9	40.4
10	39.3
11	43.1
12	41.5
13	41.2
14	29.3

Table 2

an example of this performed on the 13U chassis previously chosen as the EUT.

Test method

The single piece of empirical data used for this portion of the system analysis is the previously mentioned *fan performance* curve. This is gathered by again utilizing an airflow test chamber, or a wind tunnel, to characterize an air mover's ability to overcome a static pressure situation. In the case of the sample EUT the exhaust of a single blower, operating at high speed, was affixed to the airflow test chamber. Static pressure was then incrementally decreased from the maximum achievable to zero. At each increment we measured the differential pressure across the internal nozzle of the test chamber and calculated the volumetric flow rate. Table 3 and Figure 3 illustrate the results:

Static Pressure (in. H2O)	Flow Rate (cfm)
3.14	0.0
2.59	55.1
2.25	75.3
1.98	93.3
1.65	114.6
1.33	131.3
1.11	143.0
0.93	150.3
0.79	157.2
0.46	173.2
0.30	178.5
0.00	184.2

Table 3

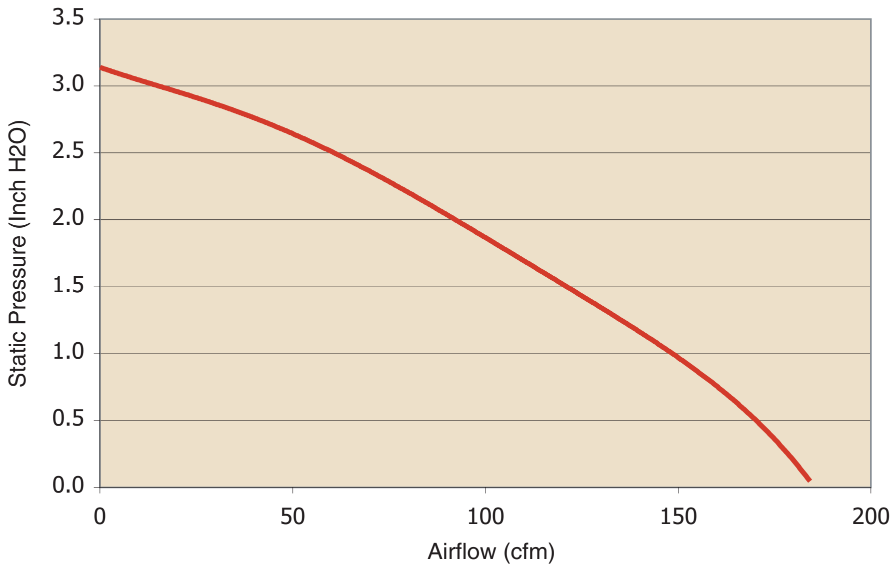

Figure 3

From this information the performance curve for the entire blower system (all four blowers working in conjunction) was derived. Since the EUT has four radial blowers working side by side, the fan law pertaining to fans in parallel operation was applicable. According to Gordon Ellison in *Thermal Computations for Electronic Equipment,* this fan law states:

> The single fan performance curve may be used to indicate the effects of using two identical fans in parallel or series (push-pull)…The parallel combination is constructed by following several horizontal constant pressure lines from zero airflow out to the fan curve. The corresponding point on the two-fan curve is at this constant pressure, but twice the airflow. If this is done for several points, a complete, two-parallel-fan curve is established.[1]

To apply this law each of the volumetric flow rate values was multiplied by a factor of four, the number of air movers in the EUT. With static pressure points for the curve all staying the same, performing this calculation yielded the adjusted system performance curve. Uniform flow through each of the EUT's 14 slots was assumed, allowing the system performance curve to be evenly divided by the number of slots to obtain the fan performance curve for a single slot, or in other words, the slot fan flow curve.

As required in the standard, this was also performed for the blowers operating at low speed and for a blower failure situation. The low speed analysis was accomplished using the airflow test chamber to capture a second blower performance curve, this time with the blower running

Single Blower Static Pressure (in. H2O)	Single Blower Flow Rate (cfm)	All Blowers Flow Rate (cfm) x 4	Per Slot Flow Rate (cfm) ÷ 14
3.14	0.0	0.0	0.0
2.59	55.1	220.2	15.7
2.25	75.3	301.3	21.5
1.98	93.3	373.4	26.7
1.65	114.6	458.2	32.7
1.33	131.3	525.1	37.5
1.11	143.0	571.8	40.8
0.93	150.3	601.4	43.0
0.79	157.2	628.7	44.9
0.46	173.2	693.0	49.5
0.30	178.5	714.1	51.0
0.00	184.2	736.9	52.6

Table 4

at low speed. Again, a factor of four was used to extrapolate the flow rate data to obtain the system blower performance curve. Next, that result was then divided evenly among each of the 14 slots in the EUT. To calculate the effect of a fan failure on the system performance curve, the single blower performance curve was multiplied by a factor of three instead of four to account for the missing blower. The EUT fan controller intelligence instructs the remaining functioning blowers to elevate to high speed in the event of an air mover failure, so for this process the curve for a single blower operating at high speed was used.

Table 4 and Figure 4 show the calculations and slot fan flow curve for the EUT operating at high speed.

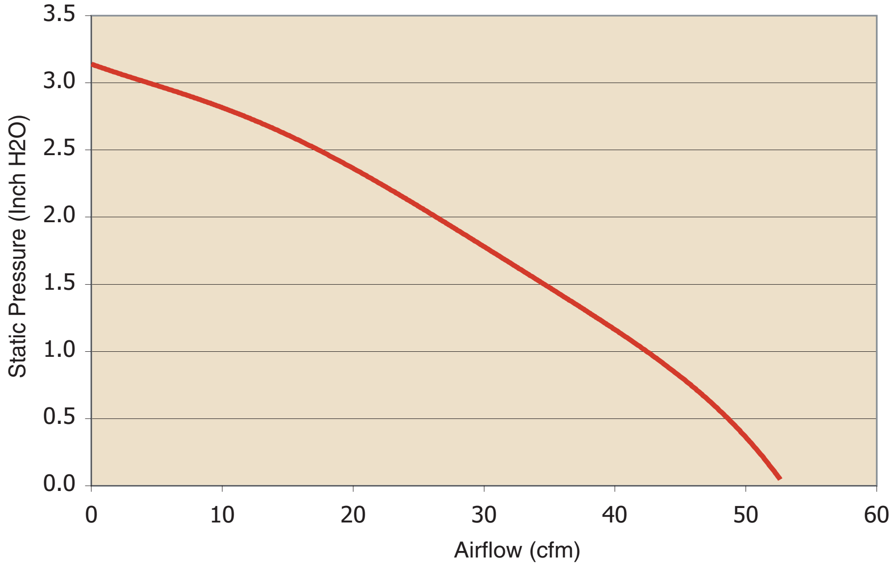

Figure 4

Again, this test method utilizes an assumption, the uniformity of the chassis' airflow distribution. However the analysis surrounding this assumption is performed on the empirically derived air catch data, making the test method acceptable for the PICMG standard. The validity of the method aside, it would be seemingly difficult to take laboratory measurements capturing the airflow performance of a single slot with varying impedance levels without an elaborate test setup. Another possibility for obtaining this type of focused data would be to default to the usage of Computational Fluid Dynamics (CFD) to measure only a cross section of the chassis. However even through CFD, empirical bulk airflow data would still be necessary as the basis of the analysis. Not to mention that the analysis and the assumptions used in the previously described test method would be exchanged for the multiple assumptions that accompany CFD studies.

Conclusion

The methodologies discussed here cover only a portion of the thermal requirements

of the PICMG standard. The complement is the requirements placed on the AdvancedTCA board manufacturers. From the perspective of the board manufacturers the goal is to create boards with a successful layout that allows for proper functionality under all operating conditions. This challenge is managed, as previously stated, through layout and by utilizing other cooling solutions such as heatsinks. It is the goal of this open format standard to bridge these two technical entities to create an environment of totally interchangeable components and ultimately complete technological interoperability between chassis and shelf vendors.

__Jason Leboeuf__ has a BSME degree from Worcester Polytechnic Institute and is the laboratory manager at IQS, an engineering services company focusing on thermal management, regulatory compliance, reliability, and mechanical engineering design of electronic products. Jason's previous work experience includes designing thermal solutions for telecommunications products at Ascend Communications and Lucent Technologies.

References

[1] G. Ellison, "Thermal Computations for Electronic Equipment" Van Nostrand Reinhold Company, 1984

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						•			www.cd4power.com
									www.camb-innov.com
								•	www.gavazzi-computing.com
									www.catapult.com
									www.celestica.com

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Centralp Automatismes											•											
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Chroma ATE											•			•								
Chroma Systems Solutions														•								
C-MAC of America			•					•	•													
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Continuous Computing									•		•			•								
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Cooler Master																						
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CTS	•																					
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									www.fairchildsemi.com
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		•							www.fujikura.com
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									www.gdca.com

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GE Fanuc Automation			•								•											
General Dynamics														•								
General Micro Systems																						
Geotest										•	•											
GESPAC					•				•													
Globe Manufacturing Sales																			•			
GNP	•					•					•											
Gompf Brackets																		•	•			
Hapco																		•				
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Hartmann Elektronik	•		•	•																		
Hirose Electric																						
Hitek Power													•	•								
Hoffman									•													
Honda Connectors																						
Hybricon			•	•	•		•	•	•	•	•		•	•		•		•	•			
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I-BUS					•						•											
ICP America											•											
Inova			•						•					•								
Integrated Device Technology			•																			
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Keystone Electronic	•																					
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Knurr USA									•		•											
Kontron	•		•								•											
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Leader Tech																		•				
LSI Logic																						
LV Power														•								
Macrolink											•					•						
MagneTek													•	•								
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MarekMicro			•																			
Martek Power														•								

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				•					www.gefanuc.com/embedded
									www.gdcanada.com
				•					www.gms4vme.com
									www.geotestinc.com
				•					www.gespac.ch
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									www.martekpower.com

Company Name	Backplanes							Chassis					Power			General						
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Measurement Computing										•	•											
Mektron Systems									•		•					•						
MEN Micro											•											
Mercury Computer Systems																			•			
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Purcell Technologies																		•	•			
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Radian Heatsinks																						
RadiSys Corp											•											
Radstone Embedded Computing											•					•						
Rancho Technology																						
Raycon Technology																						
Red Rock Technologies																						
Renesas Technology America																						
Rittal			•		•			•	•	•				•					•			
SAE Power														•								

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									www.measurementcomputing.com
									www.mektron.co.uk
									www.menmicro.com
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•									www.micro-technic.com
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Saelig																						
Sanmina-SCI								•			•	•										
SBE																						
SBS Technologies	•								•		•	•								•		
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Star Case Manufacturing										•												
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Switching Power														•								
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Universal Air Filter Co.																						
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Visionpower Ltd.														•								
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Westek			•								•											
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Wind River											•											
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XILINX		•																				
XP Power														•								
XTech									•										•			
Yamaichi Electronics																						
Zephyr Engineering																		•				

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				•					www.sbei.net
			•	•			•		www.sbs.com
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									www.zpci.com

Heads up! Warping graphics for helmet mounted displays in real time with 3U CompactPCI

By Lee Brown

The use of Helmet Mounted Displays (HMDs) has become common in combat aircraft and helicopters where weight and data presentation are gaining increasing importance. Now advanced ground vehicles are part of this trend, as the number of sensors and the volume of data is expanding exponentially, along with the challenges associated with reliable data presentation.

An HMD's glass visor displays graphics and sensor data. This enables pilots and operators to keep their eyes on the situation at hand rather than glancing away to view a console display, a situation that can mean the difference between life and death in threatening skies. In addition, guidance systems can be operated with movements of the pilot's head, freeing the pilot to perform other critical tasks during rapidly changing conditions. The aircraft's data sensors, such as Forward Looking Infrared Radar (FLIR) and video cameras, deliver increasing amounts of high-resolution data. It has become more difficult to meet the challenge of delivering this data, overlaid with other graphics, such as maps, to the pilot in real time. Another challenge is that the final graphics display must be pre-warped to compensate for the specific curvature of the helmet's display surface such that the image looks "normal" to the pilot/operator. The good news is that advanced graphics processors and very high bandwidth interfaces can be used to ensure real-time HMD performance. Even better, small form factor 3U CompactPCI provides a low-weight, compact platform ideal for space constrained cockpit environments.

HMDs are complex systems that normally consist of many functional elements, one of which captures video data from sensors such as FLIRs and cameras. Next the HMD analyzes the captured data and overlays it with graphics data. Following analysis and overlay, the HMD must warp the combined graphics and video data to compensate for the curvature of the helmet glass onto which the final image is presented. Because the characteristics of the glass are unique from helmet to helmet, warping algorithms also vary depending on the display surface being used. The process of preparing the combined video data for presentation is further complicated by whether a monocular, binocular, or single merged display system is being used, with most systems now using dual eye image systems. The Helmet Mounted Display system provider as well as the physical helmet itself faces all of these challenges.

In HMD system design, timing is everything. The pilot's safety depends on the display of sensor and graphics data in real time. Adding to the system designer's difficulty is the fact that the images are typically coming from the outside world, which is visible to the pilot, so the smallest delays (system latency) are very apparent to the pilot. This means that the latency of video data coming through the system must be reduced to the greatest extent possible. Unfortunately, traditional HMD systems demand multiple time-consuming processes. These multiple processing stages typically require additional hardware and the real estate typically found on 6U+ size boards, a major obstacle for weight and space constrained fighter jets and helicopters. Adding to all of the electronic, video, and optical challenges faced by HMD system suppliers, there are the physical challenges of the helmet itself. The objective is to keep the helmet lightweight and provide a simple connection to the electronics box driving it. These challenges led designers to adopt digital video interfaces rather than the traditional analog interfaces, as these provide low power, simple helmet electronics, and compact, lightweight cabling to the helmet. With the need to maintain low latency and the problems of passing digital video through bulkheads, it makes sense to locate the electronics unit driving the helmet in close proximity to the pilot: the HMD electronics chassis are typically mounted in the cockpit area or under the pilot's seat. Because the physical electronics box needs to be quite close to the pilot's helmet, the HMD chassis size and weight must be minimized. The positioning of the electronics unit however does not reduce the environmental conditions that it needs to withstand. Even a cockpit environment can be harsh, depending on the platform. For example, the large gun mounted underneath an attack helicopter cockpit makes it subject to violent shock and vibration. While the environmental aspects can be improved through ruggedization, the main challenge of getting all of the electronics into a box that fits into a fairly small space makes the 3U form factor the preferred choice for system designers.

The significant challenge with the HMD systems is to be able to acquire the different forms of video data, process them, supply them to the graphics function, overlay graphics, and then warp the result prior to display on the helmet. Figure 1 (courtesy of BAE Systems) shows a typical advanced HMD. In many HMD systems, different boards within the system perform these different functions:

- Video acquisition
- Video processing
- Overlaying of graphics
- Warping

The serial nature of the process tends to add multiple frames of undesirable latency to the video. Many systems use dedicated hardware to mix the graphics and video, then separate hardware to support the often-complex warping algorithms on the combined image. The warping hardware can take the form of commercial hardware such as that found in projection televisions. These multiple stages lead inevitably to latency issues.

Combining the functions

A superior solution minimizing latency and providing state-of-the-art performance,

Figure 1

such as that used in the Curtiss-Wright CCA-730 3U CompactPCI card, is to combine all of these functions into a graphics processing module providing a very high performance Visual Processing Unit (VPU) and multiple high performance CPUs (Figure 2). This approach requires a very high bandwidth interface pipe to deliver the high resolution sensor video data directly into the module and onto the VPU. The VPU then overlays the graphics and performs the warping function using the performance of the VPU and the flexibility of OpenGL. While most graphics processing modules use PCI as the interface to the GPU/VPU, this would be insufficient for a high performance HMD system with high resolution streaming video being received. For this reason, the CCA-730 Imaging Platform uses high performance 8X AGP and state-of-the-art PCI Express interfaces to provide the high bandwidth data path into the GPU/VPU, supporting FLIR and camera data acquisition in real time and without any loss of video quality.

Curtiss-Wright's first generation of ultra high performance HMD Imaging Platform, the CCA-728, provided advanced graphics and general purpose processing capabilities on a single 3U CompactPCI

Figure 2

based module. The second generation card, the CCA-730, provides a significant increase in both graphics and general purpose processing while reducing power and making use of industry leading interface standards such as PCI Express. For applications with less demanding video bandwidth and performance requirements, a cost effective HMD system can be designed using PCI based graphics modules such as the Curtiss-Wright PMC-704 card. However the trend is toward more and more incoming video arriving for processing. HMD systems are being tasked to process larger amounts of data as sensors are becoming much more capable. In addition, the resolutions that they generate have become much larger. This

puts additional pressure on the graphics subsystem to capture and process the higher resolution video. On many newer platforms, incoming video formats can be as large as 2K x 2K pixels, with HDTV formats of 1920 x 1080 pixels becoming increasingly used.

To handle the greater video bandwidth, the 730 features two backplane interfaces, one a PCI Express data path that uses a standard high bandwidth multigigahertz capable ERNI connector, and the other a standard CompactPCI interface. The CompactPCI bus communicates with the other I/O boards in the HMD system. The PCI Express interface receives the streaming video from the other boards within the system that are receiving the video from the sensors. The data comes through the PCI Express interface and is transferred directly into the memory of the GPU/VPU, where the graphics overlay and warping takes place.

Another important element of a high resolution HMD system is the integrity of the data being presented. Figure 3 shows what the pilot sees (photo courtesy BAE Systems). Increasingly, pilots have become dependent on the video from their helmet displays, resulting in the criticality level of the HMD system increasing. A failure in the HMD system can be critical. For example, if due to a failure of the system, the graphical data on the helmet fails to be updated, or "freezes" for some finite period of time, this condition may not be obvious to the pilot for a finite period of time. In a combat situation, this delay can be life threatening. Similarly, a blank screen can leave the pilot without crucial data. Two leading solutions ensure fault tolerance. One option is to employ rigorous development processes such as DO-254 for the hardware and DO-178B for the software. This typically adds many millions of dollars to the development costs and when standard commercial state-of-the-art components are used, a "freeze" condition may still not be detected. While Curtiss-Wright offers both DO-254 and DO-178B solutions, we also support a hardware based Video Integrity Monitoring (VIM) solution. The VIM is able to detect a freeze condition within one-sixtieth of a second. Moreover, the VIM can alert the system and the pilot that the data being displayed is frozen. The VIM would typically be used in conjunction with other system integrity solutions, but could also provide a cost effective standalone solution for some systems.

> "On many newer platforms, incoming video formats can be as large as 2K x 2K pixels, with HDTV formats of 1920 x 1080 pixels becoming increasingly used."

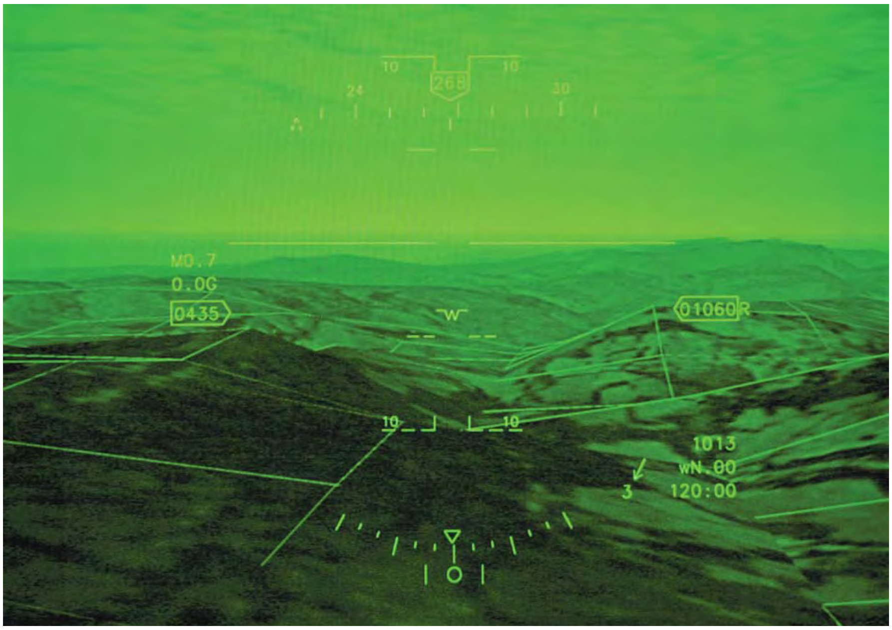

Figure 3

Because HMD systems are typically deployed in harsh environments, the 730 package is highly ruggedized. Designed to meet Level 200 ruggedization (-40 ºC to +85 ºC), the card shown in Figure 2 comprises a 3U CompactPCI base card and a mezzanine, utilizing Curtiss-Wright's advanced conduction cooling capabilities to manage the combined power dissipation. The host and mezzanine card fit into a one-inch slot pitch.

Conclusion

HMDs provide a great example of an application where several technology trends have come together, in this case the proliferation of high-resolution data, the demand for smaller and lighter systems, and the need for real-time processing and display of complex graphics and video. Each of these trends on its own would formerly present a difficult obstacle to overcome. But through the combination of the latest generation of VPU/GPU and a highly integrated and ruggedized 3U CompactPCI form factor, the challenge was not simply met but was far exceeded.

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Taking embedded, open systems technology to new heights in earth orbit space applications

By Doug Patterson

With recent developments in COTS design and execution, it is no longer necessary to depend upon expensive purpose-built computer designs to withstand the extreme demands of earth orbit and deep space applications for onboard subsystems such as flight guidance and navigation, communications support, data handling, and robotic manipulator functions.

Today, space-qualified open systems COTS single board computers and modules tailored to the varying demands of space environments are delivering the same cost- and time-saving, 3U CompactPCI-compliant solutions as their earth-bound predecessors. These include industry-standard, off-the-shelf solutions delivering better than five times higher performance at one-half the weight and one-third the cost of previous purpose-built computers designed for space applications.

Using the CompactPCI bus interface in these COTS subsystems for space applications enables standardized, off-the-shelf solutions that are able to fit in smaller physical configurations. This ability to downsize physical systems without compromising functionality can reduce the overall weight and lower launch costs. Plus, as a standardized COTS solution, it offers flexibility for rapid, near-immediate software prototyping, coupled with a quick and affordable platform for customization or expansion.

Confronting new challenges to COTS designs

The economy of open systems COTS designs has been recognized, accepted, and proven time and again in ruggedized solutions for demanding military applications. But the unique attributes of the space environment create demands exceeding the capabilities of even the most stringent MIL-SPEC ruggedization levels. These attributes include:

Radiation levels

As a major concern in space applications, requirements for radiation tolerance can vary widely based on orbit elevations – with levels as low as 10-20 Krads for low earth orbit elevations, to greater than 100 Krads of radiation tolerance in Geostationary Earth Orbiting (GEO) and some deep space applications. The angle of inclination of the spacecraft orbit also influences radiation tolerance requirements. Exposure to these levels of radiation can affect electronic circuits in a variety of ways, including single event upsets, latent defects, latchup, and charge trapping/charge drain. Volatile memory subsystems are also particularly susceptible to the effects of radiation.

> "Protection, capable of functioning in less than one 10,000th of a second, is needed to protect the computing microelectronics through the use of crowbar Silicon Controlled Rectifiers (SCRs) on the main power lines."

Extreme temperature cycling

This can include temperature swings from near absolute zero to levels of 200 °C or more, as a satellite rotates in orbit from cold to direct sunlight conditions several times a day.

Vacuum

Relatively high levels of vacuum (on the order of 1E-4 Torr) can trigger problems with drawing out any volatile materials and/or trapped gasses from, for example, plastics, lubrication greases, and component packages. That can potentially lead to corrosion of some internal electronics or fine-tolerance mechanical components and the degrading of contamination-sensitive instruments such as optics.

Shock and vibration

While systems operating in a space orbit environment might not encounter any more shock or vibration problems than an earthbound system, the stresses of space vehicle launch require appropriate levels of ruggedization for embedded system components.

A checklist for radiation-tolerant space module design

Uninterruptible operations are important to the computations performed for critical events in many functions. To ensure reliability in the space radiation environment, radiation-tolerant devices are critical for multiple system functions, including:

- Processor, memory, and system controller (PCI bridge and memory controllers)
- User programmable timers and/or counters
- A safety watchdog management subsystem to an external radiation hardened watchdog supervisor
- Reset mechanisms
- CompactPCI bridge
- All mitigation schemes

Combining high reliability radiation-hardened components with alternative circuit designs and thorough testing can

deliver rugged board solutions that achieve a Total Ionizing Dose (TID) tolerance of > 100 Krad. The result is the ability to tolerate a wide range of threats to system reliability, such as:

Single event upsets
These occur when a high-energy particle (an ion, electron, or proton) changes the state of a gate or flip-flop at random. Error Detect and Correct (EDC) or Error Check and Correct (ECC) capabilities with built-in redundancy help to catch those occurrences and let the system run with either corrected data or with an alternative hardware subsystem.

Latent defects
These can be caused by particle impacts that alter the crystalline boundaries or energy barriers on an ongoing, cumulative basis until the part fails catastrophically.

Latch-up
This is caused when a heavy particle (like a neutron) hits the base semiconductor and causes the normally reverse-biased thyristors embedded in the substrate as part of the wafer fabrication process to suddenly avalanche and conduct. Protection, capable of functioning in less than one 10,000th of a second, is needed to protect the computing microelectronics through the use of crowbar Silicon Controlled Rectifiers (SCRs) on the main power lines. This keeps the power supply charge from burning out everything downstream in the event of the sudden power surge.

Charge trapping/charge drain
This condition occurs when particles impinge on IC floating gates that are designed to accumulate a trapped charge, like those used in nonvolatile Flash memory devices. An ion can hit a gate's charged storage site, which can potentially add or drain charge and alter the data stored in that device, flipping the stored data from a 1 to a 0 or vice versa. Either way, this represents corrupted data.

Choosing a rad-tolerant processor

At the core of any COTS embedded system design intended for space applications is its microprocessor. A Silicon-On-Insulator (SOI) PowerPC microprocessor with internal, parity-enabled L1 and L2 cache memory offers the attributes necessary to deliver unparalleled performance in the space environment – with throughput of more than 1500 Dhrystone MIPs. SOIs offer high performance, as well being low power and radiation-tolerant. An inherent benefit of the SOI process is that this family of microprocessors is tested and flight-qualified to meet and exceed all levels of radiation hardness. Additionally, its inherited latchup-immune feature provides uninterruptible performance over an extended period of time when operations are critical.

Protecting volatile RAM memory subsystems

Memory devices are particularly sensitive to space-based effects. For example, depending on the space environment, random access memories such as SDRAM can be particularly prone to flipping bits or erasure.

A number of strategies can be implemented to protect onboard volatile memory resources from radiation and ensure

reliable mission operations with onboard flight software, as has been shown by proton and heavy-ion testing on various device types.

Majority Vote Truth-Table

A	B	C	V
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Majority Voter Circuit

(The logic gate representation of the majority voter.)

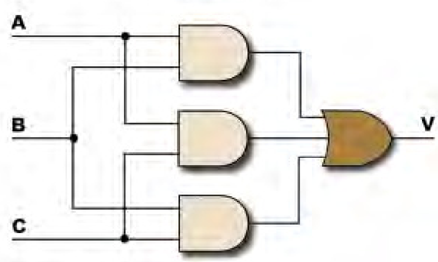

Figure 1

For SDRAM applications, used heavily in providing instructions and data to the processor, one of the most effective techniques for maintaining data integrity takes advantage of triple redundancy with hierarchical voting mechanism logic incorporated in a radiation-hardened FPGA. For radiation hardness and reliability at the component level, the SDRAM controller can be implemented with a majority-rule, triple-voting mechanism in anti-fuse FPGAs (as opposed to SRAM-based FPGAs). Along with three physically separate banks of SDRAM, the volatile memory is demonstrated to meet high performance and radiation tolerant operations. To maximize performance, this voting mechanism cannot introduce any processor fetch-wait states. This circuitry must run "silently" in the background until it detects a bit error, and correct this bit error before the data is presented and latched into the processor. The circuit must also capture this correction event and present this data to the processor for future processing as the criticality of the application sees fit. Figure 1 demonstrates the basic concept of this triple-voting mechanism.

Protecting nonvolatile Flash memory

Handling multiple functions, such as in-deployment mission program updates, within a single board computer in space typically requires redundant software modules and multiple configurations. To maintain multiple boot images of the different software modules and configurations typically handled by a single board computer, a reliable nonvolatile memory is needed to provide reconfigurability and adaptability. Protecting the integrity of the extensive firmware utilities stored in this memory – typically Flash – is essential to successful mission operation.

Boot Flash capabilities can be protected by dual redundancy such as using two independent banks of boot Flash, for example, in combination with a watchdog mechanism. Providing redundancy in this way enhances the opportunity to boot successfully after initiated or environment-induced resets – such as a software reset, a power cycle reset, or a single event functional interrupt.

Reliable NOR Flash can be used to store the user's application, along with data such as static data tables or digital filter coefficients, to deliver optimum performance for such random access scenarios. The NOR Flash can be further enhanced with an ECC correction algorithm integrated with the Flash memory controller as part of an anti-fuse FPGA.

Additional enhancements for performance and reliability

In addition to the implementation of radiation-tolerant designs within major components, numerous other physical enhancements are now available in space-qualified COTS designs and products to compensate for added demands and conditions encountered in space applications.

- Mechanical enhancements to COTS boards, such as custom metal frames, can be used to provide excellent rigidity and shock resistance. Additional mechanical shielding of the system platform provides supplemental radiation shielding, plus protection against micrometeorites.
- Conduction-cooled form factors per VITA 30.1-2002, with custom heat sink modules and metal framing provide for optimal heat dissipation and added board strength.
- Shielding and localized ovens (small heaters) can be used to maintain the long-term stability of oscillators despite extreme temperature cycling, increasing their reliability and reducing frequency drift.
- Special conformal coatings are available to protect assembled components and minimize potential problems of outgassing caused by the high vacuum levels in space.
- Full-range temperature certification from –55 °C through +85 °C is achievable with 100 percent pretesting, characterizing, and screening of all active and passive components, and 100 percent radiation testing and characterization of finished rad-tolerant boards and integrated subsystems.

Parts selection – a critical factor for success

While the physical demands of manned and unmanned space vehicle applications require the highest reliability and certifiable radiation tolerance, sadly, the general availability of MIL-STD-883B components is dwindling toward oblivion. And even designing and building a COTS board or subsystem to defense application standards is not the preferred solution.

Each batch of semiconductors utilized to construct space-qualified COTS modules has some level of process variation that affects each device's overall transistor gains, etch boundaries, and well depths which, in turn, affect speed, performance, and radiation tolerance. Unfortunately, probability batch testing of single devices or the characterization testing of one board does not certify a space-qualified design. In fact, these are great examples of *random samples of one* that make it hard to draw a valid conclusion.

Each component used in each design must be individually tested, certified, and tracked against each component's lot and date codes, with full documentation and traceability. Components that are characterized must – by definition – be from the exact same lot and date code. If not, that completely nullifies the testing. On the upside, performance and certification of characterization tests can increase both predicted and actual radiation tolerance levels to nearly five times those of unscreened devices. Therefore, the need for safety margins far outweighs the added costs.

Integrated benefits of COTS – from development to deployment

As previously discussed, other reliability issues can be addressed by building in dual redundancy or triple redundancy within the COTS board designs themselves. And while many of these mitigation techniques have been introduced individually in the past, their availability as an integrated radiation hardened solution on a single board such as Aitech's S950 (Figure 2) brings new efficiency and economy to varying requirements across a wide range of space applications. This includes everything from low-earth orbit, middle earth orbit satellites, or geosynchronous orbit satellites and robotic vehicles, to the deep-space International Space Station, to Mars, and beyond.

Finally, COTS designs also enable quick delivery, from stock, of engineering development units for custom prototyping, followed by fully characterized flight units, also available from stock. Because both are based on the same COTS design, they are 100 percent software compatible, facilitating the transition from development to deployment without changing software.

Figure 2

***Doug Patterson** is VP Worldwide Sales & Marketing, Aitech Defense Systems. He is a 20-year veteran of the computer industry. Doug has been a member of all of the industry's major standards committees.*

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SIP: Step-by-step

By Alan Davison

In the modern telecommunications environment, users are demanding more and more sophisticated media services and choices from their communications service providers. For example, someone might want to make a phone call sitting at their computer, which is plugged into the Internet Protocol (IP) network, and then hand over the call to their mobile phone, logged into the wireless radio network, when they need to move away from the desk. They may also wish to add video, conference in other users, or simply exchange data files. IP Multimedia Subsystem (IMS) defines an IP-based, unified network architecture that can deliver this level of seamless mobility, providing the user with ubiquitous and flexible access to all types of multimedia-based services such as Voice over Internet Protocol (VoIP), video streaming, conferencing, and data exchange, regardless of the end device or access route.

One of the key enabling components of IMS is the open standard Session Initiation Protocol (SIP), which gives a scalable, extensible, and most importantly network independent method of establishing communication sessions between two or more end users. By stepping through a basic SIP call setup, the beneficial features of the protocol become clear. Figure 1 depicts the network architecture.

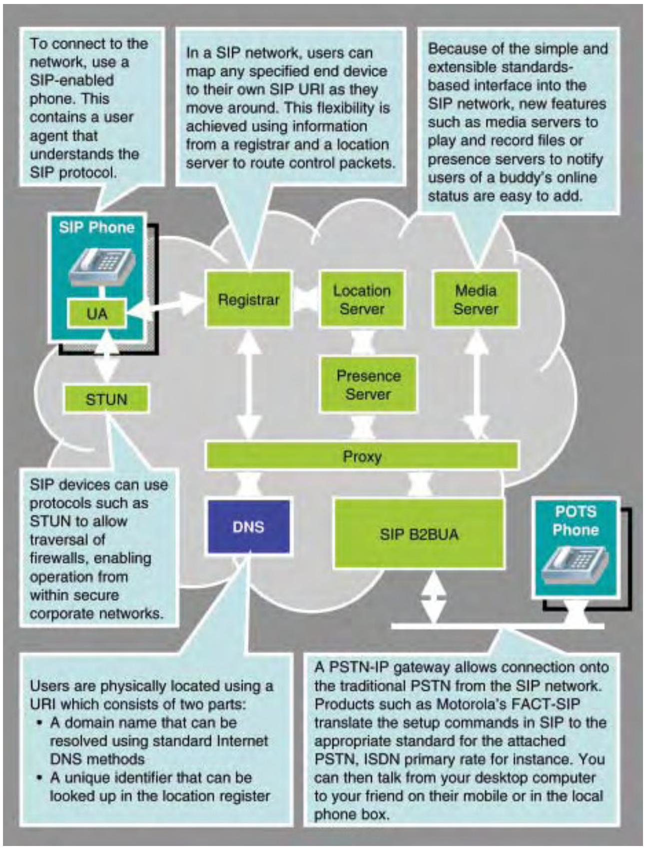

Figure 1

Making a call

Controlled and ratified by the Internet Engineering Task Force's (IETF) RFC 3261, Figure 2 describes a typical SIP call with the corresponding message sequence.

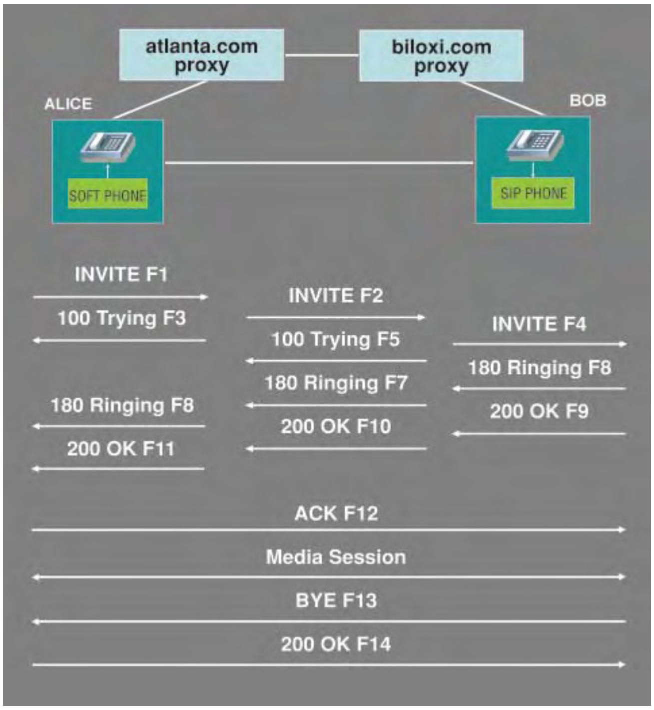

Figure 2

Breaking this down, the call (or session) initiation needs to register a device for each user and establish a data path between the two users. In addition, it must negotiate a data format to use for voice data, transmit voice data, and terminate the call.

Step 1: Registration

As already described, when a user wants to make calls using VoIP technology, they need an account (similar to having a phone or e-mail account). This gives them a unique Universal Resource Identifier (URI). For example, Bob@biloxi.com. In order to make or receive calls, the user must associate an end device such as a computer or a SIP-enabled phone with this URI. This process is called registration (Figure 3).

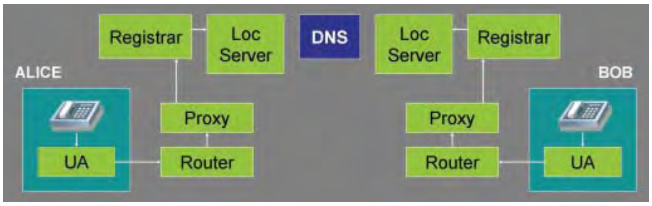

Figure 3

When Alice turns on her phone, the User Agent (UA) inside it sends a SIP register packet (containing the local IP address of the SIP phone) to her selected proxy server, which will in turn pass this to a registrar. The registrar stores the IP address and the URI in the location register for future reference. The advantage of this process is that it allows Alice to have several different devices capable of making VoIP calls without changing her public URI. She can even hand off between them. Once Bob has gone through the same process, either user may call the other one.

Step 2: Initiate a call

Alice decides to call Bob, so she enters Bob's address and initiates a call, which causes Alice's UA to send a SIP INVITE message to its selected proxy. The challenge for the proxy is to obtain Bob's IP address, so that voice data can be routed between them. This is called the SIP discovery process (Figure 4).

The SIP discovery process follows this sequence:

1. The UA adds its own address to the INVITE message (this is so the message responses can be routed back along the same route).
2. The proxy then uses the Domain Name Server (DNS) to obtain the IP address of the proxy in Bob's domain.
3. The modified INVITE message moves onto the newly resolved IP address (by default SIP proxies listen on port 5060).

Using this process allows SIP to use features of the existing functionality within the network, such as simple text-based identifiers and traffic-based load balancing.

Step 3: Resolve the URI to IP address mapping

Once the INVITE message has arrived at the correct proxy, it needs to be mapped to a specific IP address for Bob's SIP phone (Figure 5).

This is done by looking up the URI in the location register. It will then return the current IP address that Bob registered during Step 1. Now the INVITE message can finally be sent to the end device.

Step 4: Accept the call

The next problem to address before the call can be accepted is to ensure that both ends of the call are using the same data format. This is solved using information passed in another protocol called the Session Description Protocol (SDP). The SIP INVITE message from Alice also contains an SDP payload, which describes such items as the voice sample rate and compression codec supported by Alice's phone. Provided Bob's phone is compatible with one of these formats, Bob is notified that Alice is trying to call him (the phone will ring). Once he answers the phone and hence accepts the call, his IP address is sent back to Alice in a response message, along with an SDP payload containing the selected codec configuration, which then follows the same route back to Alice. She will then send an ACK message to signal the setup is complete (Figure 6).

Step 5: Send voice data

Now both parties have each other's up-to-date IP addresses, enabling them to start sharing voice data. This is normally sent directly peer-to-peer between the two endpoints (P2P) using RTP over IP. As a result, it does not travel via the same route as the control (Figure 7).

Once the session has been initialized, the job of SIP is largely done. Note that SIP messages can be sent during the voice call to update the configuration, send text messages, or even add other parties to the call.

Step 6: Terminating the call

Once Bob and Alice have finished their discussion, the call session can be terminated by hanging up in the usual manner (Figure 8).

This causes a SIP BYE message to be sent to the other party in the call, which is then acknowledged. At this point, the call has been terminated.

Conclusion

As can be seen from the proxy-based architecture and call life cycle, SIP is a simple, efficient, and highly scalable solution that is helping to meet the growing demand for VoIP communications. Large scale adoption of the protocol within the industry allows a great deal of vendor interoperability. Although not explicitly dealt with in this article, SIP network elements also allow for future expansion and the addition of new features by passing messages that contain unsupported fields transparently through to the next proxy or end user.

Evidence of popularity and flexibility of SIP are shown by its adoption as a key element in the IMS, which will be used to handle multimedia services within next generation networks.

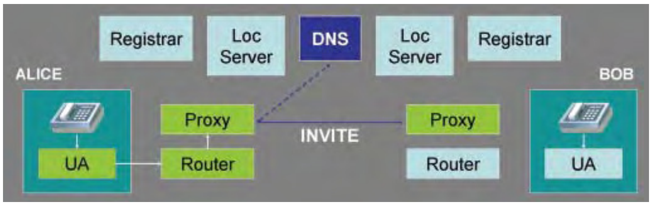

Figure 4

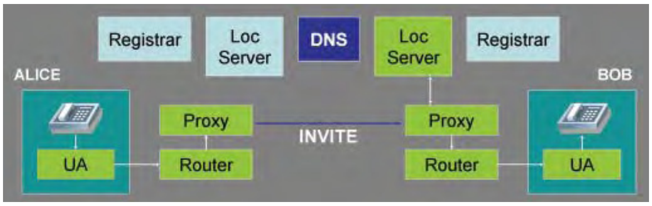

Figure 5

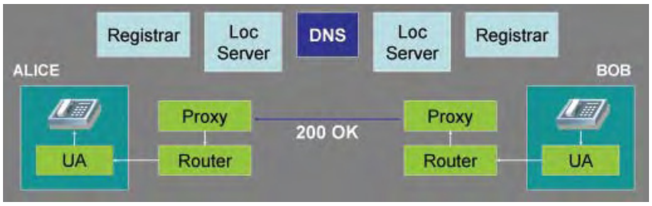

Figure 6

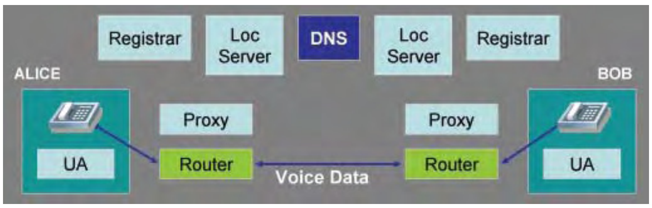

Figure 7

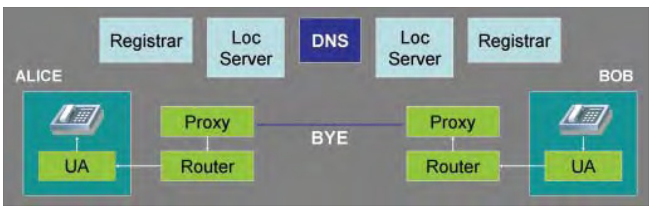

Figure 8

Alan Davison is a technical marketer for standards-based media products in the Embedded Communication Computing business of Motorola, with a focus on next generation network elements. He has spent most his career on real-time embedded DSP programming and telecom framework software. Alan has an MEng in Electrical and Electronics Engineering from the University of Nottingham.

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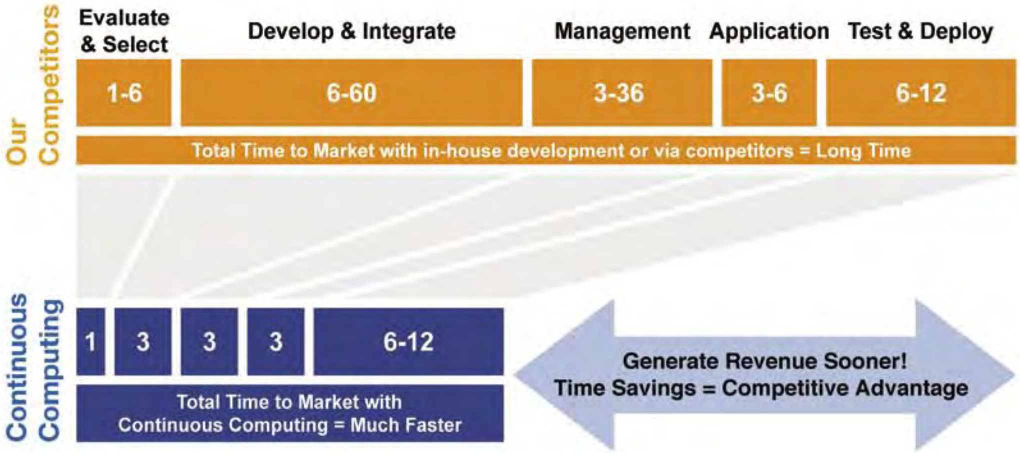

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Packet processing: Tradeoffs for performance and density

By Chuck Hill

The AdvancedTCA family of specifications offers the telecom industry a Commercial Off-the-Shelf (COTS) environment for future system development. One area that has been the domain of proprietary systems is the data plane. The data plane demands a high level of functionality and density, often requiring highly specialized implementations.

Today's data plane is dominated by platforms with Application Specific Integrated Circuits (ASICs). Network processors promised to do for packet processing what Digital Signal Processors (DSPs) did for signal processing: provide a programmable environment for rapid product deployment. But network processors came with their own set of challenges.

A new class of packet processors looks to provide a more conventional development environment, while providing specialized features for high density and performance. They offer the ability to deploy more complex applications more quickly, at a competitive price point.

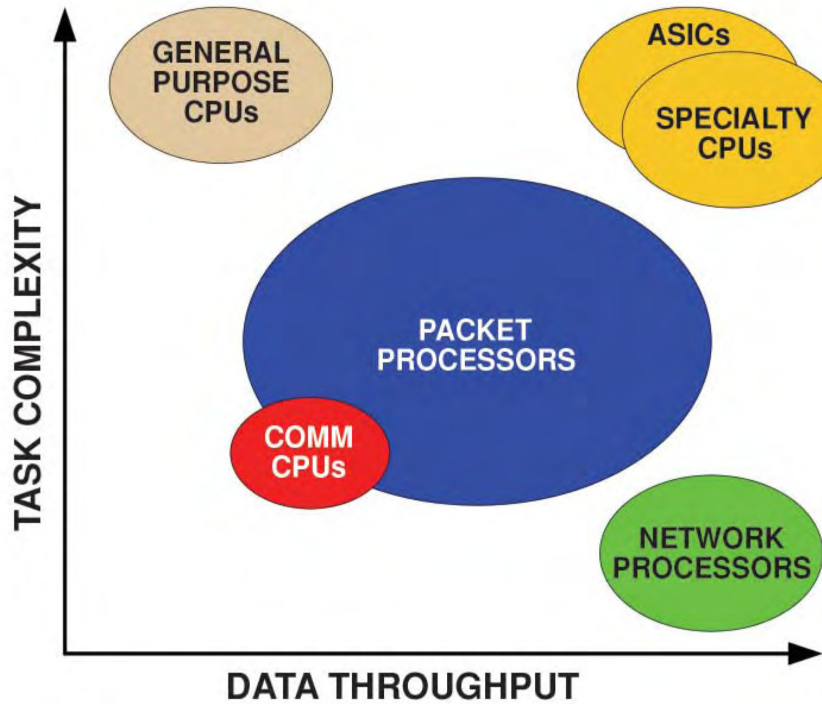

Figure 1

The processing landscape

Today's designers have an abundance of choices for processing their applications. Selecting the right processor depends on a number of factors including performance, cost, and development time. The landscape (see Figure 1) is very complex with many choices, but some generalizations can be made:

General purpose CPUs are most commonly found in control plane and server applications. Designers can choose from a variety of RISC and CISC architectures such as x86 and PowerPC as well as from a price/performance range that extends from embedded microcontrollers to high-end server-class CPUs.

General purpose CPUs support the highest complexity tasks, with multiuser operating systems and sophisticated development tools. When using a standard operating system environment like Linux, general purpose CPUs can provide an environment where applications can be developed and deployed rapidly.

But general purpose CPUs lack resources for high data throughput. Usually data must traverse a peripheral bus, a *Northbridge*, and a front side bus to enter the CPU. These buses are optimized for compute performance, and not necessarily for streaming data. So, as a relative comparison, general purpose CPUs are most optimal for complex tasks, and least optimal for high data throughput.

Network processors are almost the exact opposite of general purpose processors. Most network processors contain a variety of resources for data processing including:

- Fabric interfaces
- Search engines
- Low latency memory access

The internal bus structures are designed for high throughput, low latency data applications.

But network processors are generally based on processors with specialized functionality. The micro-CPUs, channel processors, or state machines used are very good at the tasks they are designed for, and very limited at other tasks. One common limitation is instruction space. If the complexity of the task causes the code to grow beyond what can be contained in one CPU, the task has to double up on usage, cutting the data throughput in half. As a generalization, network processors handle relatively repetitive tasks at very high data throughput. If the task is a good fit for a network processor, it will provide the highest performance.

ASICs or highly specialized CPUs such as DSPs offer the ability to provide the

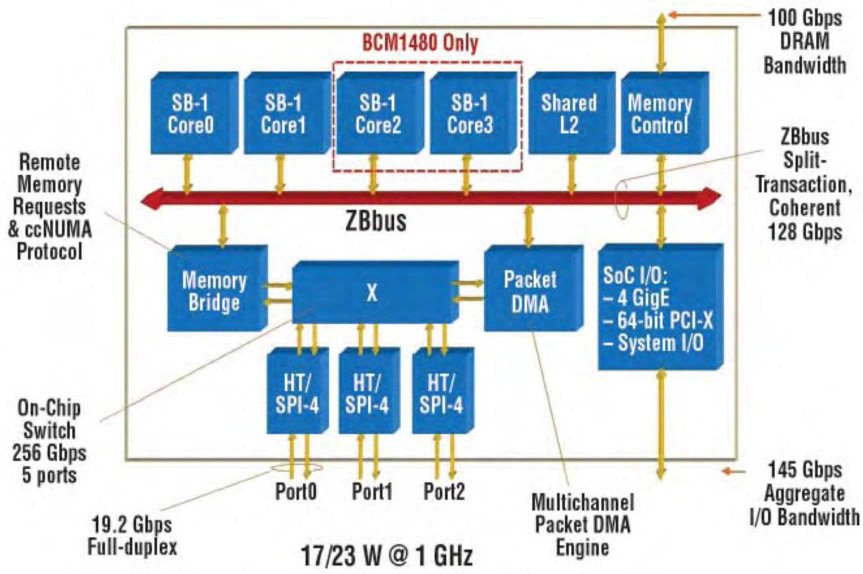

Figure 2

"But more recently companies have been putting multiple CPU processing cores in a System-on-Chip (SoC), optimized for packet processing. Cavium Networks, PMC-Sierra, and Broadcom are leading this market, but many other products are on the way."

highest performance for any range of complexity. However these devices are highly specialized, and often part of a company's proprietary intellectual property. That level of development is not feasible for many companies.

Packet processors bend features

Right in the middle of the spectrum is a relatively new class of processor generically called a packet processor. A packet processor is based on a more general purpose processing core, but is structured for use in data processing applications. The processing cores support linear instruction spaces, and include features like L1 and L2 caches, but are not as superscalar as a high-end general purpose CPU.

Packet processors are not new. They have been around in the form of a smaller cousin often referred to as a communication processor. Communication processors usually combine a specialized communication unit with a general purpose CPU. The Freescale PowerQUICC processor is an example of a communication processor.

But more recently companies have been putting multiple CPU processing cores in a System-on-Chip (SoC), optimized for packet processing. Cavium Networks, PMC-Sierra, and Broadcom are leading this market, but many other products are on the way.

An example of the blending of features in an SoC is the Broadcom SiByte BCM1480 (Figure 2). The BCM1480 combines:

- Four 64-bit RISC processor cores with a memory controller
- L2 cache
- Four Gigabit Ethernet MACs
- A host of peripherals
- Three-port high-speed packet interface

The three high-speed data ports can be configured as HyperTransport interfaces for processor-to-processor connections, or as SPI4.2 interfaces for direct input of 10 Gbps data into the SoC. The integration of high-speed ports with an on-chip switch is what makes the BCM1480 an interesting choice for packet processing applications.

It's all about the software

The real differentiator for packet processors is application development. The 64-bit RISC cores in the BCM1480 are programmable the same way any general purpose CPU is. The BCM1480 runs a standard Linux operating system, and uses the same C/C++ development tools, allowing applications to be quickly developed and debugged.

But like most general purpose CPUs running an OS, performance is not always optimal. For more optimal packet throughput, the application can be profiled (again with standard tools) and the critical path functions can be offloaded to specific CPU cores running a real time OS, or even simple firmware. That can result in as much as a 5x improvement in packet throughput.

The ability to develop under a standard OS, and then selectively optimize for performance, gives implementers the best of both worlds. They can get a rapid time to market for early trials, and achieve very competitive performance densities. In contrast, network processors require the application to be optimized and partitioned from the beginning. And while the tools for NPs are getting better, application development still requires specialized skills and a significant learning curve.

Packet processing blades

AdvancedTCA supports up to 200 W per slot. The combination of the high amount of integration and low power dissipation of the BCM1480 allows for up to four BCM1480s to be combined in a very high performance packet processing blade. Continuous Computing's FlexPacket™ is one example of a packet processing blade that is optimal for applications including:

- Access control routers
- Session border controllers
- VPN gateways
- RNCs
- SGSN
- GGSN
- IPTV streaming video systems

FlexPacket ATCA-BCM40 combines multiple 1480s with a variety of mezzanine sites that allow the blade to be configured for different I/O needs, or to add various coprocessing resources like security processors. The BCM40 can support data rates beyond 10 Gbps with significant application complexity.

***Chuck Hill** is a system architect for the Technology Office of Continuous Computing. He has 11 years experience designing fault tolerant and high availability systems for the telecom market. Chuck Hill has participated in developing several PICMG specifications. He has a master's degree in engineering and a master's degree in business.*

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Telecom				General											Voice		Wireless			
General	OC-3/STM-1	T1/E1/J1	T3/E3	Gateways	Hot swap	Interfaces	Embedded Internet	Modem/Fax modem	Optical	Remote access	Routers/Switches	Servers	TCP/IP	Turnkey system	General	VoIP/VoP	General	GSM/GPRS	SDR	Website
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BWI				•										•								
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Carlo Gavazzi Computing Solutions														•								
Catalyst Enterprises																						
CES		•		•																		
Cirpack																						
Clovis Solutions, Inc.																				•		
Cluster Labs				•									•									
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Cogency Technology				•																		
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Comtech AHA Corporation																						
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Datalight																						
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Diversified Technology																						
DNA Enterprises																						
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Fairchild																						
Fine Point Systems																						
Fortinet				•																		

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Telecom				General											Voice		Wireless			
General	OC-3/STM-1	T1/E1/J1	T3/E3	Gateways	Hot swap	Interfaces	Embedded Internet	Modem/Fax modem	Optical	Remote access	Routers/Switches	Servers	TCP/IP	Turnkey system	General	VoIP/VoP	General	GSM/GPRS	SDR	Website
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Foundry Networks																						
Fulcrum Microsystems																						
GAO Research																					•	
GE Fanuc Automation		•		•					•					•								
General Micro Systems				•										•								
General Standards														•								
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GNP								•													•	
GoAhead Software																				•		
H.A. Technical Solutions																						
Hilscher Gesellschaft																						
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Telecom				General											Voice		Wireless			
General	OC-3/STM-1	T1/E1/J1	T3/E3	Gateways	Hot swap	Interfaces	Embedded Internet	Modem/Fax modem	Optical	Remote access	Routers/Switches	Servers	TCP/IP	Turnkey system	General	VoIP/VoP	General	GSM/GPRS	SDR	Website
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MOSCHIP																•						
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Telecom				General											Voice		Wireless			
General	OC-3/STM-1	T1/E1/J1	T3/E3	Gateways	Hot swap	Interfaces	Embedded Internet	Modem/Fax modem	Optical	Remote access	Routers/Switches	Servers	TCP/IP	Turnkey system	General	VoIP/VoP	General	GSM/GPRS	SDR	Website
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Signalogic																						
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Software components at play in a COTS world

By Oren Teich

The next generation of carrier grade communications equipment is placing unprecedented demands on the software layer. The latest trends in high-speed interconnect technologies and next generation processors, along with improved reliability, manageability, and serviceability all demand advanced operating system and middleware support. In the same way that these trends have pushed hardware towards a more open Commercial Off-the-Shelf (COTS) platform, they are driving software vendors to provide open, standards-based, and scalable platforms. Here Oren reviews the software components at play in a COTS world, and identifies the key points to consider when choosing a vendor.

Communication networks are different from other kinds of computing applications. Such networks require both very high reliability and extremely high performance. Not only must they process large volumes of data at high speeds, but they must do so while limiting downtime to minutes per year. Failures can have huge economic consequences and can even result in the loss of a human life. In 1991, a packet-switched network failed and caused hundreds of millions of dollars in losses. It knocked out air traffic control in the New York City region for more than eight hours and disrupted 85,000 travelers. This single example is enough to illustrate the detrimental impact such network breakdowns can cause.

Building communication networks that are reliable and perform well presents both business and technology challenges. The physics, finances, and computing are often state-of-the-art. The information and communication market segment is experiencing revolutionary changes, as demand for both fixed-line and mobile access increases and users move from narrowband to broadband channels. Telecommunications equipment manufacturers and service providers need scalable and extensible solutions to enable them to keep pace with this growth while offering competitive products and services that take advantage of new technologies.

The proportion of network functionality being implemented in software is continually increasing. Typical networking applications are gateways, bridges, routers, signaling servers, and management servers. Such applications are sophisticated, complex, and very expensive to design, so it makes economic sense to provide a common set of software services that such applications can use as a foundation to build upon.

AdvancedTCA includes specifications for boards, shelf management, and firmware. Standards-based blade modules increase port and compute density. They reduce complexity and power consumption and create common platforms. At the same time a standardized, intelligent platform management interface enables automated and highly efficient blade-, shelf-, and system-level management capabilities. Together, these advancements create an architecture that vastly reduces solution footprints to a fraction of historical deployments, all the while providing powerful solutions with greater computing capacity and the ability to help reduce operating costs.

The same trends that are driving the COTS revolution on the hardware side are pushing software developers to standardize. Developers are increasingly turning to open source software solutions for the

application-ready carrier grade platforms they require to build and deploy communication network infrastructure systems. These environments require high performance, scale, and availability, but the need to reduce time-to-market and total cost-of-ownership is driving service providers to adopt open source technologies. Industry accepted carrier grade features and rock solid, peer reviewed engineering, combined with the convenience, rapid innovation, and simplicity of open source, make a truly compelling value proposition. These are crucial advantages in deploying cost-effective carrier grade systems to the market.

In this open building block design, middleware is the critical piece in managing all resources, thereby enabling expected levels of dependability. The Service Availability Forum (SAF) interface specifications are the critical glue that binds the open pieces together. To combine best-of-breed solutions in this environment, it's vital that you choose software components that not only provide the functionality required, but also embrace both the spirit and intent of the open standards.

Driving software standards

Several requirements for availability and serviceability point to work from the SAF to define Application Programming Interfaces (APIs) and architecture for application and hardware availability and management. Details can be found in the SAF Application Interface Specification and the SAF Hardware Platform Interface Specification. These requirements specify services and corresponding APIs for hardware platform management and for application failover. The application services are:

- Cluster Membership Service
- Checkpoint Service
- Event Service
- Message Service
- Lock Service

The management structure for these services is the Availability Management Framework. Each service and framework has a corresponding API. The management of the hardware in SA Forum specifications is covered under the Hardware Platform Interface.

MontaVista Software became the first commercial software vendor to support the Application Interface Specification v1.0. This support includes the APIs that comprise the Cluster Membership Service and the Availability Management Framework, which includes application heartbeat and failover APIs. This capability has been open sourced by MontaVista Software and is rapidly adding further services defined by the SA Forum. The project is hosted at http://developer.osdl.org/dev/openais.

Successful adoption and deployment of AdvancedTCA depends on a strict commitment to standards and interoperability. Development within the Open Source Community, including members from commercial and noncommercial entities, is the best process for ensuring such requirements are met. The community is committed to driving standards to ensure interoperability and consistency in the services that are required across multiple telecom solutions, thus allowing for telecommunication equipment manufacturers to leverage the benefits of COTS to reduce costs and speed time to market while focusing on their value-added services.

Oren Teich is responsible for MontaVista's worldwide product management. With over seven years of Linux experience at leading technology companies, Oren has been working with some of the very first commercial Linux companies in both marketing and engineering roles.

Prior to MontaVista, Oren worked at Sun Microsystems, Cobalt Networks, an Internet radio company, Vixie Systems, and US West. Oren has a BS in Computer Science from the University of Colorado, Boulder.

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Fax: 408-328-3875
E-mail: oren@mvista.com
Website: www.mvista.com

Company Name	Development					Prototyping						Software													Website
	Dev. platform	Development tools	IDE	Reference system	System integ. svcs.	Boundary scan	Bus analyzer	Debugging aids	Emulator	Fabric analyzer	JTAG	Application	BIOS	Board support pkgs.	Compilers	Development tool	Driver	Java	Library	Linux	Modeling tool	Networking	Operating system	Protocol stack	
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	Development					Prototyping						Software													
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Corelis								•																	www.corelis.com
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Systems designers' dreams become reality with AdvancedMCs

By George Kontopidis

Advanced Mezzanine Cards (AdvancedMCs) appear to be on the way to creating a market bigger than all PCI Mezzanine Cards (PMCs) and other daughterboards combined. There are two main reasons this is likely to occur – AdvancedMCs have the right scale for a hot-pluggable Field Replaceable Unit (FRU) and they leverage AdvancedTCA standardization work. AdvancedMCs will most likely replace proprietary functional modules at a high enough volume so that the economies of scale and their ubiquitous use in the telecom sector will drive costs to commodity levels. Just think what will happen if a good fraction of the 1.7 billion mobile subscribers start using a chain of AdvancedMCs in Node Bs, RNCs, and gateways, extending to multimedia transcoding processing elements.

A philosophical shift

Traditional board designers included expansion options to accommodate unplanned functionality and future needs. The terms piggyback and daughterboard are indicative of this concept – both imply that they supplement a base board with more functionality. AdvancedMCs, however, have caused a shift in the I/O expansion philosophy. The new concept is that the mezzanines are the main functional units. The minimal functionality provided by the "big" base board is simply the interconnectivity of these new, more powerful cards. Instead of CPUs with piggyback I/Os, now the concept is I/Os with processing capability on AdvancedMCs. Components evolving quickly with more functionality can now be located on replaceable units, not on large, hard-to-replace base boards. Generic backplanes with carrier blades managed by generic frameworks can outlive multiple generations of silicon when implemented on AdvancedMCs. Whether using Advanced Telecom Computing Architecture (AdvancedTCA), MicroTCA, or blade server shelves, you can now bring a new level of functionality to your system without the expensive forklift upgrades of the traditional telco industry.

The right scale

Silicon functionality has been increasing according to Moore's Law. At the same time, the physical size of chips remains small, due in part to advances in the packaging of small ball grid arrays. These forces combine to make it possible to design highly functional modules in an AdvancedMC footprint. It's possible to fit just the right number of communication elements on an AdvancedMC, either for the access plane or the edge plane of the network. If too many elements are packaged in an FRU, the point of failure becomes a concern. However, if too few elements are packaged together, the cost of interconnects becomes a concern. For these reasons, a typical AdvancedTCA blade is too big to serve as an FRU, while AdvancedMCs are just the right size.

Manufacturing organizations also prefer multiple, smaller, printed circuit boards versus larger boards such as AdvancedTCA. Using high volumes of smaller boards:

- Reduces assembly prices
- Simplifies inventory management
- Improves manufacturing yields
- Makes assembly corrections simpler
- Reduces packaging and shipping costs

Minimal premium for high availability

One of the significant advantages to building systems using AdvancedMCs rather than full AdvancedTCA blades is the ability to create inexpensive, highly available systems. To illustrate the cost advantage, consider building a redundant 1,536-port video gateway system using full-size AdvancedTCA blades. Rough calculations indicate the need for 2:1 redundancy for AdvancedTCA blades and 6:2 redundancies for AdvancedMCs. Under reasonable assumptions you can derive that the AdvancedTCA system implementation is more than 50 percent more expensive than the equivalent AdvancedMC implementation, as illustrated in Figure 1. Of course,

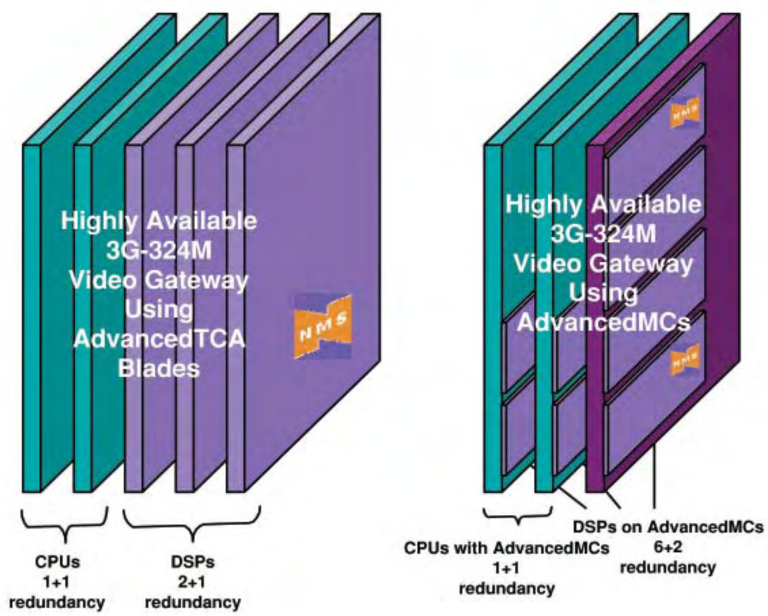

Figure 1

such a cost difference becomes smaller if the desired port size is a multiple of the ports that can fit on an AdvancedTCA blade, and that cost difference eventually diminishes as the size of the system becomes very large.

Packaging flexibility

The cost of common equipment is often a factor in choosing the best packaging solution for a telecom system. Given that shelves require a processing unit – and most likely two for high availability, the minimum system requires at least two AdvancedTCA slots for CPUs. For an entry-level system supporting market trials of a new service, an AdvancedMC with I/O trunks can be added on the same CPUs without occupying another slot. Alternatively, system designers can consider replacing full-blade CPUs with their AdvancedMC counterparts, located on one or two carrier blades. Additional AdvancedMC slots can be used for peripheral I/O elements for early-stage capacity expansion. The four standardized sizes of AdvancedMCs (half- or full-height and single- or double-width) provide further flexibility for expansion to CPUs and carrier blades.

Just liberate your thinking for a moment to other application spaces, such as IT blade servers or remote access servers, where the cost of entry is important and graceful scalability is critical, and you'll find even more examples for which using AdvancedMCs provides a packaging advantage.

Panels for access

As AdvancedMCs become the main functional unit, they require onboard I/O as well as external connectivity to minimize system-level connector transitions. This, plus the need for mechanical handling of FRU insertion and extraction, led to a nice AdvancedMC front-panel design. And for the hardcore 23-inch rack designers in North America, the option remains to connect T1 lines to the back of the shelf using Rear Transition Modules, feeding the carrier blades and the hosted AdvancedMCs.

Management inheritance

The PICMG group spent significant time on the Intelligent Platform Management Interface (IPMI) subsystem used in AdvancedTCA shelves. It represents a well designed physical and logical management layer including:

- Dual interconnects for high availability
- Payload power management to control safe amperage consumption
- Payload watch-dog and reset features for reliable operation
- Temperature monitoring to avoid thermal runaways

AdvancedMCs leverage the previous design by extending IPMI's benefits to mezzanine components. The same framework used for an AdvancedTCA chassis is used to provide negotiated power and thermal management to the granularity of AdvancedMCs.

Natural interconnects

The base and fabric switching of the AdvancedTCA backplanes have been extended naturally to the AdvancedMCs. You can now access a large bandwidth of streaming data without physical conversion to parallel buses. There is no need to slow down data rates due to skew concerns of buses and their respective latches. The new advanced silicon of CPUs, NPUs, and DSPs can now be packed on mezzanine cards with minimal glue logic. Switching of data streams is now much easier and is typically embedded in the same glue logic.

Clock is ticking

Most of us remember the MVIP, SCSA, and H.100 days in which designers needed special help with sensitive clock circuits and PLLs. This accumulated experience lead to the inclusion of TDM clocking in AdvancedTCA, which is naturally inherited in AdvancedMC designs. No more complex clock extractions or clock edge alignments every time a clock has to travel from one module to another.

According to a Crystal Cube Consulting report last year, the AdvancedMC market is estimated to become around $8 billion by 2008. Marketers say, "Interesting times we live in." Engineers say, "The good designs are just around the corner." At the end of the day, good designs, put to use in major markets, are likely to cause industry disruptions. AdvancedMCs are conceived thoughtfully and will lead to cost-efficient system designs and target large and growing markets.

__George Kontopidis__ is the senior vice president of Products and Technology Strategy at NMS Communications. He has been managing development activities for the telecom industry for the past 18 years. He has a PhD and MSEE from the University of New Hampshire, and he is a member of the IEEE and ACM.

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Company Name	Carriers										Mezzanines											Website
	AdvancedMC	IP	IP (Intel.)	M-Module	PC/104	PC•MIP	PMC	PMC (Intelligent)	TIM	Other	CCPMC	IP	M-Module	PC•MIP	PCI-X	PrAMC	PrPMC	PTMC	Switched fabric	XMC	Other	
4DSP							•										•			•		www.4dsp.com
AcQ InduCom				•																	•	www.acq.nl
Acromag		•																				www.acromag.com
ACS-Tech 80		•																				www.acs-tech80.com
ACT/Technico							•			•							•					www.acttechnico.com
Actis		•										•					•					www.actis-computer.com
Aculab										•												www.aculab.com
Adas										•												www.adas.fr
Adcom															•							www.adcomtec.com
ADLINK Technology							•															www.adlinktech.com
AdvancedIO Systems																				•		www.advancedio.com
Advantech							•			•												www.advantech.com
Alphi Technology		•	•																			www.alphitech.com
AMCC																			•			www.amcc.com
American Portwell			•																			www.portwell.com
Artesyn Communication							•									•	•	•				www.artesyncp.com
AudioCodes												•										www.audiocodes.com
BiRa		•																				www.bira.com
Brandywine Communications											•											www.brandywinecomm.com
Brooktrout										•												www.brooktrout.com
BWI			•				•															www.bwi.com
C&H Technologies		•		•																		www.chtech.com
Carlo Gavazzi CS							•															www.gavazzi-computing.com
Centralp Automatismes							•															www.centralp.com
CES	•						•										•					www.ces.ch
Comtech AHA Corporation															•							www.aha.com

Company Name	Carriers										Mezzanines											Website
	AdvancedMC	IP	IP (Intel.)	M-Module	PC/104	PC•MIP	PMC	PMC (Intelligent)	TIM	Other	CCPMC	IP	M-Module	PC•MIP	PCI-X	PrAMC	PrPMC	PTMC	Switched fabric	XMC	Other	
Concurrent Technologies						•	•	•		•												www.gocct.com
CorEdge Networks, Inc.	•																					www.coredgenetworks.com
Critical I/O							•															www.criticalio.com
Curtiss-Wright Embedded		•					•															www.cwcembedded.com
DRS							•															www.drs.com
DSS Networks															•		•					www.dssnetworks.com
Dynamic Engineering		•					•															www.dyneng.com
EKF-Electronik						•				•				•								www.ekf.de
Embedded Planet																•	•	•				www.embeddedplanet.com
esd																	•					www.esd-electronics.com
EuroTecH							•															www.eurotech.it
Evergreen Group							•															www.evergreengrp.com
Extreme Engineering							•	•			•						•			•		www.xes-inc.com
GD California										•												www.gdca.com
GE Fanuc Automation							•								•		•					www.gefanuc.com/embedded
General Micro Systems							•															www.gms4vme.com
GESPAC										•												www.gespac.ch
GNP										•												www.gnp.com
Hilscher Gesellschaft							•															www.hilscher.com
Inducom Systems													•									www.acq.nl
Innovative Integration							•															www.innovative-dsp.com
Inova										•												www.inova-computers.de
Intel							•															www.intel.com
Interface Concept							•										•					www.interfaceconcept.com
Interphase	•						•											•				www.interphase.com

Continued on page 76

Company Name	Carriers										Mezzanines											Website
	AdvancedMC	IP	IP (Intel.)	M-Module	PC/104	PC•MIP	PMC	PMC (Intelligent)	TIM	Other	CCPMC	IP	M-Module	PC•MIP	PCI-X	PrAMC	PrPMC	PTMC	Switched fabric	XMC	Other	
Kane Computing																	•					www.kanecomputing.com
Kontron							•									•					•	www.kontron.com
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MEN Micro				•		•								•							•	www.menmicro.com
Mercury Computer Systems														•			•					www.mc.com
Motorola																	•					www.motorola.com/computing
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Prodrive																	•					www.prodrive.nl
RadiSys Corp							•										•					www.radisys.com
Radstone Embedded Computing							•			•	•											www.radstone.com
RT Logic!																	•					www.rtlogic.com
Sabtech Industries							•															www.sabtech.com
SANBlazeTechnology							•															www.sanblaze.com
SBE							•											•				www.sbei.net
SBS Technologies		•				•	•				•			•		•	•				•	www.sbs.com
SEAKR Engineering											•											www.seakr.com
Spectrum Signal Processing							•														•	www.spectrumsignal.com
Sundance									•								•					www.sundance.com

Company Name	Carriers: AdvancedMC	Carriers: IP	Carriers: IP (Intel.)	Carriers: M-Module	Carriers: PC/104	Carriers: PC•MIP	Carriers: PMC	Carriers: PMC (Intelligent)	Carriers: TIM	Carriers: Other	Mezzanines: CCPMC	Mezzanines: IP	Mezzanines: M-Module	Mezzanines: PC•MIP	Mezzanines: PCI-X	Mezzanines: PrAMC	Mezzanines: PrPMC	Mezzanines: PTMC	Mezzanines: Switched fabric	Mezzanines: XMC	Mezzanines: Other	Website
Surf Communication																		•				www.surf-com.com
Technobox							•			•							•				•	www.technobox.com
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SHB Express: The next big thing in passive backplanes and slot boards

By Jim Renehan

Did you know that the origins of PICMG began with several companies coming together to develop the first open standard for industrial computers using slot boards and passive backplanes? The industry standard that resulted from this initial specification effort was called PICMG 1.0, which set the stage for many new and exciting developments in passive backplane and slot board technology.

As new technologies and standards evolved, the terms *passive backplanes* and *slot boards* came to mean different things to different people. For our purposes, we will restrict the use of the term *slot board* to describe Single Board Computers (SBCs) or System Host Boards (SHBs) that use edge connectors to plug into backplanes (passive or otherwise) used in PICMG 1.3 or SHB Express systems. In this article we'll focus on SHB Express systems and discuss applications, market size, and the technology differences of PICMG 1.0, 1.2, and 1.3 (PICMG 1.x) slot board SBCs/SHBs and backplanes.

Slot board SBCs and backplanes cover a broad range of applications in diverse markets such as military/aerospace, industrial automation, communications, medical, and instrumentation. The major advantage of PICMG 1.x SBCs and backplanes is that these systems effectively support multiple option board slots (PCI Express, PCI-X, PCI, and ISA), fast Mean Time To Repair (MTTR) and flexible backplane slot configurations. One of the distinct advantages offered by PICMG 1.x systems is the ability to take advantage of the plethora of commercially available off-the-shelf plug-in option boards. Choices abound in the types of option boards available to meet various system design requirements. The numbers and choices of option boards available in the slot board form factor will keep PICMG 1.x system implementation options viable for the foreseeable future. Figure 1 illustrates a "typical" chassis populated with a PICMG 1.3 system host board and a backplane with PCI Express, PCI-X, and PCI option board slots.

The slot board SBC and passive backplane market is a diverse and constantly evolving market. You may find that surprising given all the attention focused on newer PICMG 2.x and PICMG 3.x technologies. That's understandable because it's easy to get excited about new specifications and markets, and bypass the tried and true technologies represented by PICMG 1.x.

Several market studies state that growth for PICMG 1.x products has remained steady and should continue that way over the next several years. Figure 2 illustrates a respectable growth rate for PICMG 1.x products from 2004 through 2008. In the base year of 2004, total US market shipments for PICMG 1.x SBC/SHBs and backplanes were likely around the $218 million mark, with 2008 shipments estimated to grow to $270 million. Granted this isn't the "billions and billions" of

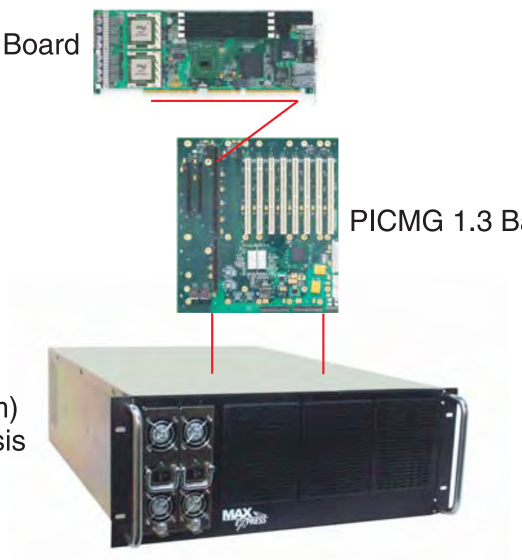


Figure 1

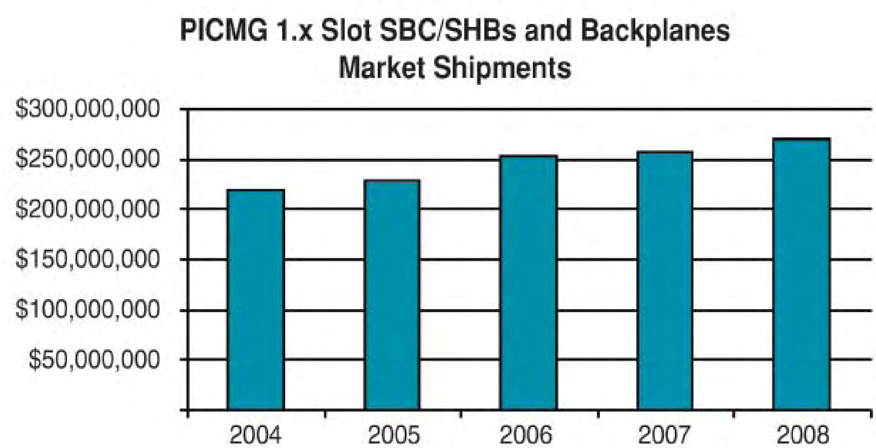
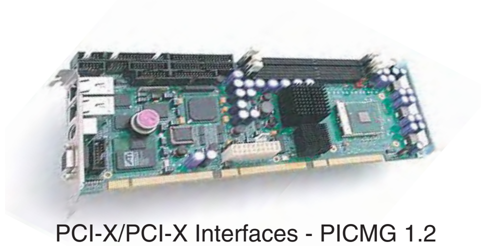


Figure 2

dollars associated with other technology markets, but these are "real" numbers based on years of shipping data and market observations. When comparing board-only shipping data, PICMG 1.x products represent a respectable portion of 2004 embedded computing shipments.

SHB Express/PICMG 1.3 represents the latest innovation in the PICMG 1.x market. SHB Express is a new industry standard, recently adopted by the PICMG membership, and replaces the PCI/ISA, PCI-X parallel bus single board computer-to-backplane interfaces used in PICMG 1.0 and 1.2 with PCI Express serial interconnects. Figure 3 shows the evolution of PICMG 1.x slot board to backplane interconnects.

PCI/ISA Interfaces - PICMG 1.0



PCI-X/PCI-X Interfaces - PICMG 1.2

PCI Express Interfaces - PICMG 1.3

Figure 3

With the speed of today's processors and chipsets the data bottlenecks tend to be moving out to the peripheral I/O. The PICMG 1.0 standard defines PCI/ISA parallel bus interconnects between the single board computer and backplane. PICMG 1.2 increased the data throughput speed between the SBC and backplane by replacing the ISA parallel bus with the PCI-X parallel bus. This helped the data bottleneck issue a little bit but did not address the root cause of the problem: parallel bus technology. PICMG 1.3 addresses the inherent limitation of parallel bus technology by replacing the PCI/ISA and PCI-X/PCI-X interfaces with multiple, scalable, full-duplex, PCI Express links between the system host board and the backplane. The term SHB was used in developing the PICMG 1.3 specification in order to make a clean break between the parallel bus technology of PICMG 1.0 and the scalable serial interface technology offered by PICMG 1.3. Functionally speaking the SBC and SHB accomplish the same basic tasks in their respective PICMG 1.0, 1.2, and PICMG 1.3 systems. Often the terms SHB and SBC are used interchangeably. Figure 4 compares the peak available bandwidth capabilities of PCI/PCI-X parallel bus interfaces and PCI Express (Gen. 1).

The PICMG 1.3 specification defines some interesting features that can be implemented by the compatible SHBs and backplanes. Optional I/O can be routed through the SHB's edge connector C and down to the backplane in order to

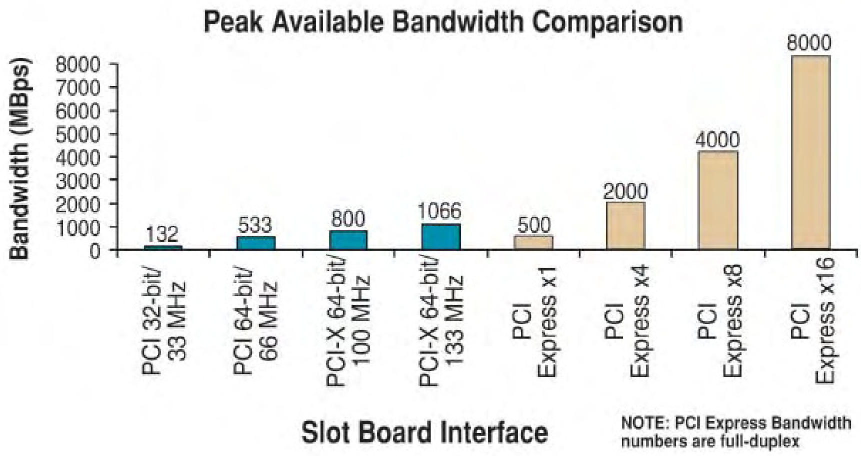


Figure 4

decrease MTTR by moving some cable connections from the SHB down to the backplane. The optional I/O capabilities defined in the specification include:

- Four USB
- Dual SATA
- Dual 10/100/1000BASE-T Ethernet

Soft power control implementations in PICMG 1.0 and 1.2 systems were always a bit tricky. SHB Express addresses this inherent limitation by defining Advanced Configuration and Power Interface (ACPI) functionality support in the specification. An SHB Express system can support various soft power control/wake states associated with the ACPI control signals.

The SHB Express specification also defines Intelligent Platform Management Interface (IPMI) and Geographic Addressing (GA) signal placements on the SHB's edge connector. These signals could be utilized in a PICMG 1.3 system to implement advanced system functions like IPMI and Hot Swap in a slot board and passive backplane system. This represents a future capability since today's slot boards do not typically support IPMI and GA. Typically, this functionality has been restricted to AdvancedTCA systems, but SHB Express puts the "hooks" in place to support this key system capability in the PICMG 1.3 form factor.

One of the design advantages of PCI Express is that far fewer signal pins are required than older ISA/PCI/PCI-X parallel interfaces. This allows us to provide additional edge connector contacts for SHB power and signal grounds. The net result is that we can have the +12 V auxiliary power cable(s) plug into the PICMG 1.3 backplane and route the power signals and grounds over to the SHB edge connector slot. This new capability simplifies the power cable connections and helps decrease MTTR by moving the power connectors off the SHB and down to the backplane.

The SHB Express specification is very flexible in terms of PCI Express implementations. The specification allows for up to 20 PCI Express links between the SHB and backplane. These links can be configured in a variety of different ways. The number and type of PCI Express links routed from the SHB to the backplane is largely dependent on the type of chipset used on the SHB.

Graphics class and server class

SHB Express system host boards and backplanes fall into two broad categories: Graphics Class and Server Class. A graphics-class SHB has one x16 and either one x4 or four x1 PCI Express electrical connections to the backplane. Graphics-class backplanes have one PCI Express option board slot "plumbed" with a x16 electrical interface and several x1 board slots or one x4 slot.

Server-class SHBs and backplanes are designed to maximize the number of high-bandwidth PCI Express connections. A typical server-class SHB may have a combination of x8 and x4 links routed to the backplane. The PCI Express board

slots on a server-class backplane are electrically configured as x8 or x4 slots.

The PCI Express option board slots on any PICMG 1.3 backplane may mechanically support boards with interfaces greater than that which is electrically supported. In most cases, PCI Express's auto-negotiation capability will automatically establish communication between the SHB and the option board. Link configuration straps between the PCI Express backplane board slots and the SHB are defined in the specification for system host board designs that may not support the auto-negotiation capability.

With available bridge technology, SHB Express backplanes and SHBs support PCI Express, PCI-X, and PCI option boards. Believe it or not, there is still a demand to support ISA slots on the backplane, which can be accomplished with the use of PCI-to-ISA bridge technology. However, the cost justification of migrating an older board technology to a newer technology can be prohibitive. Figure 5 shows two examples of PICMG 1.3 backplane designs.

Conclusion

The only sure bet in the world of technology is change, and the SHB Express specification is built to support this reality. The PCI Express technology that you can purchase on the open market today supports the Gen 1 implementation of PCI Express with its signal frequency of 2.5 gigabits per second (Gbps) per lane and per direction. Option boards and chipsets will soon be available with PCI Express Gen 2 with double the signaling frequency. Advanced Switching adds additional functionality to the PCI Express protocol layers to enable advanced fabric network capability. When developing the SHB Express specification, the PICMG 1.3 Technical Subcommittee took these upcoming technology advancements into consideration. As a result, SHB Express supports both current and future iterations of PCI Express technology, including Advanced Switching. The good news is that SHB Express products support past, present, and future slot board technologies while enabling a seamless and cost-effective transition to PCI Express and Advanced Switching.

Jim Renehan is director of marketing for Trenton Technology and has held various application engineering and product management positions in the industrial automation and embedded computing industries. Jim holds a BS in Industrial Education and Technology from Iowa State University.

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Graphics-Class PICMG 1.3 Backplanes

Server-Class PICMG1.3 Backplanes

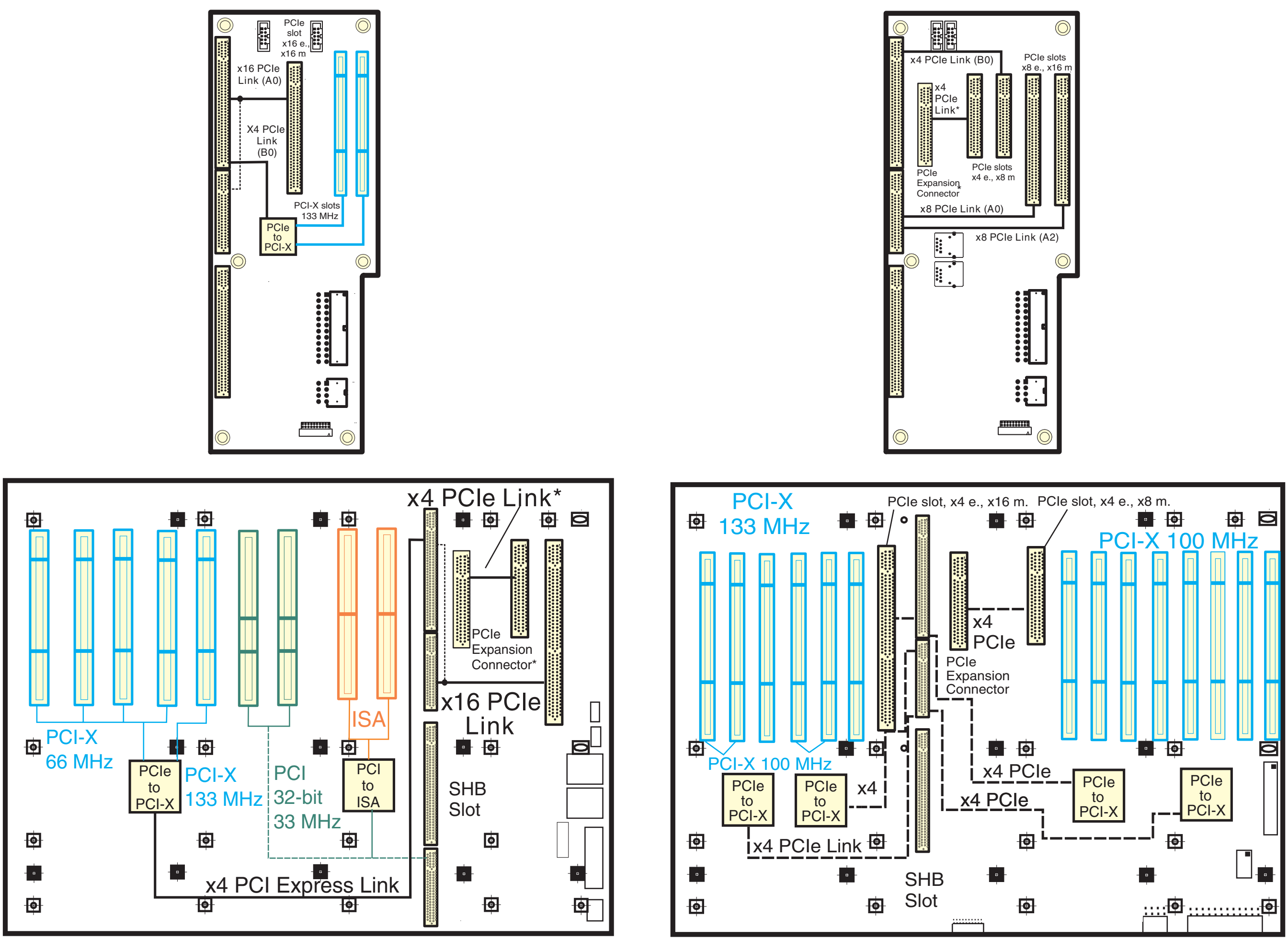

Figure 5

BUYER'S GUIDE: Board Level

Company Name	Bridge									Chips and Cores												DSP resource boards							
	cPCI-to-cPCI	cPCI-to-PCI	cPCI-to-VMEbus	PCI-to-PCI	PCI-to-PXI	PCI-to-VMEbus	Processor-to-PCI	VME-to-PCI	Other	ARM	Bridging	Bus interface	DSP	FPGA	IP	Media SoC	MIPS	Pentium	Power	PowerPC	Other	CompactPCI	IndustryPack	M-Module	PC/104	PCI/ISA	PMC	Resource boards	TIM
4DSP														•								•					•		
AcQ InduCom																						•							
Acqiris																													
Acromag														•															
ACT/Technico																													
Actel														•															
Actis																													
Aculab																						•							
Adas																												•	
Adcom																													
ADDI-DATA																													
ADLINK Technology					•	•										•													
Advantech				•																									
Agere													•																
Agilent														•															
AIM-USA																													
Aitech Defense Systems																													
Alacron																						•					•		
Alpha Data														•															
Alphi Technology																						•							
Altera Corporation														•															
Amtelco												•																	
Anatel																										•			
Andor Design																													
Annapolis Micro Systems																													
APW	•																												
Astec																													
Astek Corporation									•																				
ATTO Technology									•																				
Avnet Electronics Marketing														•															
Axiomtek																		•											
BiRa																													
BittWare														•								•					•	•	
Brandywine Communications																													
BVM																													
BWI																													
C&D Technologies																													
C&H Technologies																													
California Micro Devices												•																	
Carlo Gavazzi CS		•																											
Chrislin Industries																													
Cluster Labs																						•							
Commetrex																													
Computer Modules																													
Comtel Electronics																													
Comtrol																													
Concurrent Technologies																													
Conduant																													
Connect One Semiconductors										•																			
Continuous Computing																												•	
Coreco Imaging																						•							

Continued on page 84

BUYER'S GUIDE:

DSP		General							I/O					Memory				
Algorithm	Alternative	Board access.	Component-level	LVDS	PCMCIA/CardBus	PCMCIA/PC Card	Structured ASIC	System boards	Analog	Digital	FPGA	Industrial	Multifunction	Buffer	Flash	General purpose	Reflective	Website
																		www.4dsp.com
									•		•	•			•			www.acq.nl
										•						•		www.acqiris.com
									•	•	•		•					www.acromag.com
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																		www.actel.com
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BUYER'S GUIDE: Board Level

Company Name	Bridge									Chips and Cores												DSP resource boards							
	cPCI-to-cPCI	cPCI-to-PCI	cPCI-to-VMEbus	PCI-to-PCI	PCI-to-PXI	PCI-to-VMEbus	Processor-to-PCI	VME-to-PCI	Other	ARM	Bridging	Bus interface	DSP	FPGA	IP	Media SoC	MIPS	Pentium	Power	PowerPC	Other	CompactPCI	IndustryPack	M-Module	PC/104	PCI/ISA	PMC	Resource boards	TIM
Curtiss-Wright Embedded		•		•																									
CyberResearch																													
Cyclone Microsystems																													
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Kontron																													

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BUYER'S GUIDE:

DSP		General							I/O					Memory				
Algorithm	Alternative	Board access.	Component-level	LVDS	PCMCIA/CardBus	PCMCIA/PC Card	Structured ASIC	System boards	Analog	Digital	FPGA	Industrial	Multifunction	Buffer	Flash	General purpose	Reflective	Website
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Lattice Semiconductor Corporation																			•		•								
LAVA Computer Manufacturing																													
LSI Logic													•																
Lyrtech																						•							
Mango DSP																						•					•		
Measurement Computing																													
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DSP		General							I/O					Memory				
Algorithm	Alternative	Board access.	Component-level	LVDS	PCMCIA/CardBus	PCMCIA/PC Card	Structured ASIC	System boards	Analog	Digital	FPGA	Industrial	Multifunction	Buffer	Flash	General purpose	Reflective	Website
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CompactPCI Express: Protecting CompactPCI investments made over the last 10 years

By Andrew Brown

Very recently, the CompactPCI Express specification was finalized and made public for both 3U and 6U board formats. This standard actually permits the use of current 32-bit, parallel CompactPCI peripheral devices in hybrid slots. Hence, "old" can mix with new, bridging the generation gap, without scrapping investments in CompactPCI technology made over the past 10 years and without losing out on the obvious advantages presented by this modern serial bus architecture.

In the early 1990s, Intel developed the PCI Peripheral Component Interconnect (PCI) bus because the bus architectures of the day, Industry Standard Architecture (ISA) or Extended Industry Standard Architecture (EISA), with their industrial counterparts, SMP or ISA96, were fast coming to the end of their performance spectrum. All the more aggravating was the need to license the EISA bus. The desire for greatly improved data transfer rates and multiprocessor support spurred development of the PCI bus. In addition, when compared with the EISA bus, the costs had to be kept to a minimum without compromising user friendliness through software configuration. Since the application areas for the PCI bus were to be as wide-ranging as the technology of the time would allow, the concept had to cater to a processor-independent environment that was also license-free. What emerged was a specification with a multivendor capability that had a well-defined electrical and mechanical interface and rigid bus protocol. Upon completion of the specification, the PCI bus was handed over to the PCI-SIG, who ensured that further developments would remain multivendor friendly and license-free. Major advances to the original specification included the doubling of the data bandwidth (from 32-bit to 64-bit) and that of the bus frequency (from 33 MHz to 64 MHz). Then, in 1995, just a few years after its introduction, the standard was adopted for industry in the form of CompactPCI. Today, these properties permit maximum data throughput from 133 megabytes per second (MBps) to 533 MBps.

PCI Express, developed again by Intel, was originally termed 3rd Generation I/O (3GIO) and is a completely new bus system where data is transferred via high-speed, point-to-point serial links known as lanes. (Figure 1) In the PCI Express world, each lane comprises a pair of differential conductors with one pair for data transmit and the other for data receive. In addition, these lanes can be bundled to a maximum 32 lanes per channel. Each lane then is able to transfer data at a 250 MBps rate in each direction; with all 32 lanes bundled together, this data transfer becomes an impressive 8 gigabytes per second (GBps) (or 16 GBps in both directions) total. CompactPCI Express, by comparison, supports bus structures with 4 to 16 lanes per channel enabling data transfers up to 4 GBps. This represents a massive improvement on the current 133 MBps offered by today's CompactPCI. Compared to other parallel bus structures, CompactPCI Express is fully bidirectional, permitting simultaneous data transmission and reception, effectively doubling the 250 MBps data throughput to 500 MBps. The syntax describing this architecture is as follows: (channels) x (lanes) – so *2x4 lanes* describes two independent CompactPCI Express channels with four bundled lanes per channel. If a CompactPCI Express peripheral board cannot administer all available lanes of the system board, then the unused lanes will be automatically deactivated during initialization.

Note that the method of data transfer in a CompactPCI Express environment makes it ideal for PCB manufacture using FR4 materials, and even permits conductor lengths up to 50 cm. Being serial in nature, CompactPCI Express:

- Possesses CRC checksum algorithms for error recognition and correction
- Is AC coupled (no ground loops)
- Has native hot plug support

CompactPCI Express extension boards can be replaced without the need to remove the main power first. Because CompactPCI Express supports point-to-point connectivity only, interfacing con-

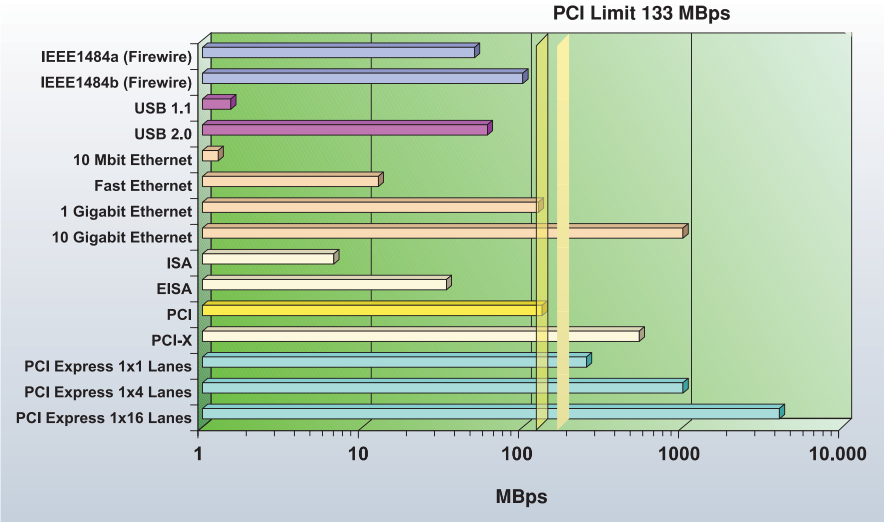

Figure 1

ventional 32-bit parallel CompactPCI boards requires *switches*. The transition between PCI and PCI Express is transparent as far as the operating system is concerned, and assuming the PCI board conforms to the PCI 2.2 specification. To use the advanced features inherent in the PCI Express standard, such as extended error handling or power management, the OS must be able to address them directly. Otherwise the existing PCI interrupts are recognized, and the device drivers remain unaltered. The first 256 bytes of configuration space are identical to the current PCI registers, and because the operating system views the PCI Express *root* or switch as a virtual PCI bridge, even older operating systems can configure CompactPCI Express devices. The BIOS must however support PCI Express completely, since such devices have a relatively large configuration space.

Capitalizing on PCI Express in an industrial environment

To take advantage of PCI Express in an industrial environment necessitated the introduction of specially tailored connectors. In total, three additional connectors have been developed to sit alongside the well-known CompactPCI connectors. Data transmission on the high-frequency channels takes place through differential Advanced Differential Fabric (ADF) connectors. These have an intrinsic impedance of 100 Ohm and an input attenuation of < 1 dB at 3 GHz. Since these connectors are used primarily for the HF signals, additional power connectors are required. These come in the form of the Universal Power Connector (UPM), which has seven individual contacts for the system board:

- One 3.3 V
- One 5.0 V
- Two 12.0 V
- Three GND

Each contact can be loaded at 15 A, which in theory at least, permits the system board to draw a maximum of 340 W. By contrast to CompactPCI, where, in general, the main board power is derived from the 5 V line, in a CompactPCI Express world the main power is drawn from the 12 V line. The core voltages on a CPU board are thus generated from it and, as a consequence, have a better signal. The –12 V signal is no longer supported on the pure CompactPCI Express slots, but is supported in hybrid configurations for legacy CompactPCI devices – assuming the PSU is capable of generating this signal.

A specially defined Enriched Hard Metric (eHM) connector is used for carrying additional I/O signals and some power. This connector is keyed, thereby preventing for example, PXI boards from being used in a configuration where rear I/O is required. In total, four different key combinations are possible defining unused I/O pins, rear I/O, extended rear I/O, PLX extensions, and bus orientated sideband signals. All combinations support Hot Swap and Wake Up functions. Except for the extended rear I/O option, additional 12 V, 3.3 V (2 A), and 5 V_{aux} (1A) power lines are available. Here, the CompactPCI Express specification deviates slightly to that of the PCI Express specification in which V_{aux} is 3.3 V and the maximum loading just 375 mA. In the CompactPCI Express specification, the 5 V signal for

Micrel's High-Voltage Hot-Swap Power Controllers – Only the Best!

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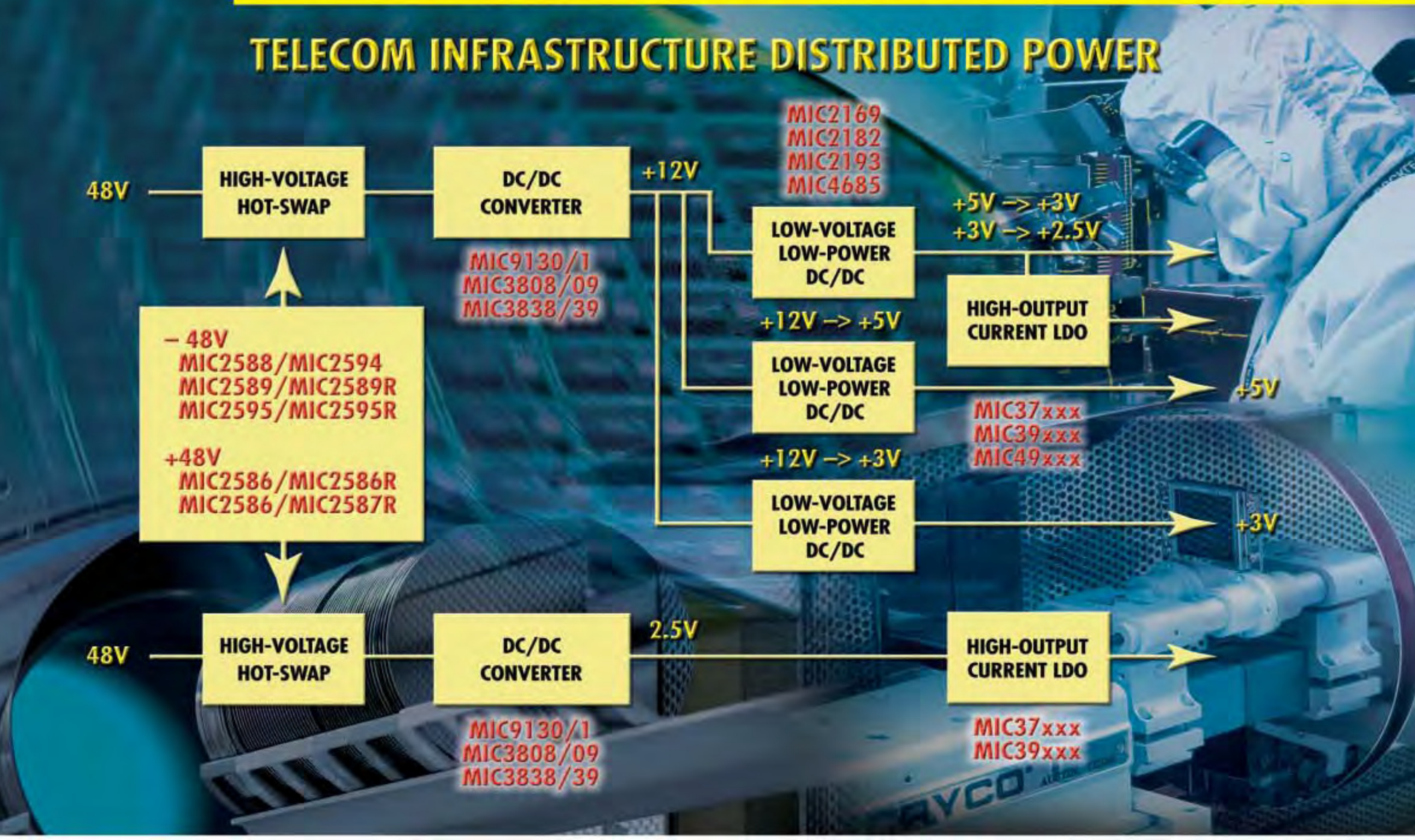

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- Open-drain, active-HIGH and active-LOW "Power-is-Good" outputs available
  - Single and multiple outputs for sequencing dc/dc converters

main board power is no longer available. In a CompactPCI Express environment, the V_{aux} is primarily used for Wake Up tasks, and is present even if the system has switched off the main power.

Two approaches apply to switching on or switching off a CompactPCI Express system. This can take place through a control signal from the PSU, or via a Wake Up event from a timer interrupt or some other external source. Here, the power consumption of the system can be regulated or reduced while in operation, allowing a CompactPCI Express system to be fully active only on those occasions where it is actually required. The second method is through the usual mechanical on/off switch. The electrical, mechanical, and climatic properties of all connectors conform to IEC-60512.

3U advantages

As with existing CompactPCI systems, all major bus signals are present in the 3U form factor, giving two major advantages over VME systems for example. One, high-performance systems can be created in a highly compact 3U format with the only restriction being the physical PCB surface area compared with the 6U systems. Given today's integration density, and serial CompactPCI Express bus system, this presents zero drawbacks. Very few contacts are required when interfacing, for example, a 64-bit parallel device. The second advantage is that those standardized extensions pertaining to telecom, for example, present in the upper region of 6U boards, do not have to be affected by the introduction of CompactPCI Express. Hence, existing standards are respected, and current installations profit from this approach.

The major changes that have taken place in CompactPCI Express compared with CompactPCI are concerned with the 3U form factor. Connectors and their use in the 6U portion remain the same and conform therefore to PICMG 2.0. It's the bus in the 3U region that has undergone the most change. Also, CompactPCI Express vastly improves upon the power consumption permitted by individual slots when compared with the requirements the PCI Express specification details. Here, for example, the power is limited by the consumption of the board occupying each slot. In the PCI Express model, power consumption is very much regulated and linked with the number of bundled lanes. So, a PCI Express board configured with 1x1 lanes can, according to the specification, consume just 10 W at startup. By comparison, in the CompactPCI Express model, the lowest power consumption at startup is in the 30 W range.

The CompactPCI Express specification defines six different types of slots that can be used in backplane manufacture. Remaining from the current CompactPCI specification are the power connector for the PSU and the *legacy slot* for existing parallel-bused peripheral boards conforming to the CompactPCI PICMG 2.0 specification. The CompactPCI Express specification introduces a number of new connectors to the system slot. Power is obtained through the seven-pin UPM connector. In addition, ADF and eHM connectors are used for the CompactPCI Express channels where they also serve the rear I/O and provide additional power outlets. The eHM connector on the system slot, need not, according to the CompactPCI Express specification, have pins allocated for power. All pins of this connector can be reserved for extended rear I/O tasks. The system slot (Master) presents the CompactPCI Express signals either as four channels, that is, 4x4 lanes or two channels with 1x8 and 1x16 lanes. As an option, a combination of 1x8 and 1x16 is also possible. However, the system slot must, under all circumstances, support as a minimum, the 4x4 lane scheme. System slots supporting 1x8 or 1x16 lanes are, in this case, only provided with 2x4 lanes. A *slotpin*, present in the system slot, defines which of the two combinations is present. The CompactPCI Express specification defines only the minimum number of PCI Express channels. Instead of, for example, the presence of the complete 4x4 lanes, at least one 4x1 lane must be present, (or in other words, one channel with at least one lane). Because the system slot does not support parallel bus architectures, a bridge is required when mapping the parallel CompactPCI bus to a single CompactPCI Express channel.

The specification allows for four different kinds of peripheral board. The first is identical to that of the current CompactPCI architecture. Then there are two pure CompactPCI Express slots and one hybrid slot in which both conventional CompactPCI connectors and Type 2 CompactPCI Express connectors are present, as Figure 2 shows. In this slot, standard 32-bit CompactPCI peripheral boards can be used or the newer CompactPCI Express boards (Figures 3A and 3B). All boards have the possibility of tapping into the eHM connector present in this slot, so that even legacy CompactPCI boards can take advantage of Hot Swap or even Wake Up functions.

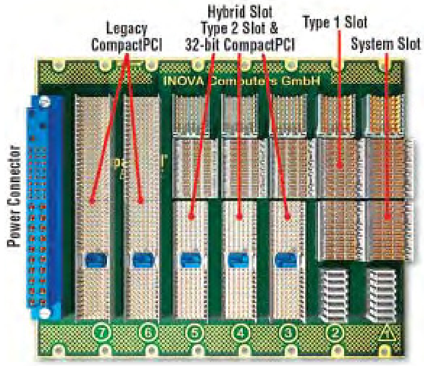

Figure 2

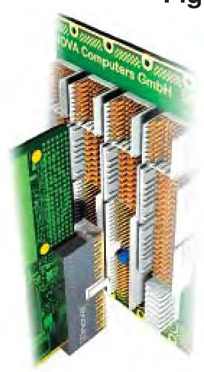
Figure 3a

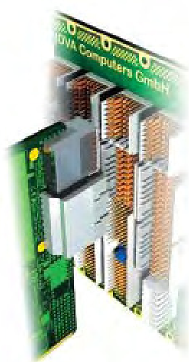
Figure 3b

The Type 1 peripheral slot has the same connector layout as the system slot with 2 PCI Express channels configured for either 1x4 or 1x16 communication. CPUs can be placed in this peripheral slot as long as they have a nontransparent bridge or are capable of Advanced Switching. Here, two PCI Express channels are present and observe the 1x4 lane and 1x16 lane scheme whereby the 1x4 lane scheme is mandatory while the second channel with 1x16 lane is optional.

Type 2 peripheral slots have ADF and eHM connectors with board power being supplied through the eHM connector only. This slot has just one PCI Express channel present with 1x4 lanes. Type 2 boards can work in a Type 1 environment but not conversely, since the UPM connector for the main power is missing in Type 2 slots. Type 1 slots are generally reserved for power-hungry boards, so the power rating of the eHM connector may not be sufficient.

By contrast to parallel bus systems where only two devices can communicate on the same bus, CompactPCI Express permits all devices to communicate simultaneously. Hence the complete bandwidth is available at all times (Figure 4).

Bridging the generation gap

The *hybrid* slot is a combination between a Type 2 peripheral slot and a traditional 32-bit CompactPCI slot. This is a universal type of slot. Either CompactPCI or CompactPCI Express can be positioned here. Even PXI architectures are supported and have their dedicated signals routed through the eHM connector. Hence, new system designs can take advantage of existing CompactPCI technology without losing out on the advan-

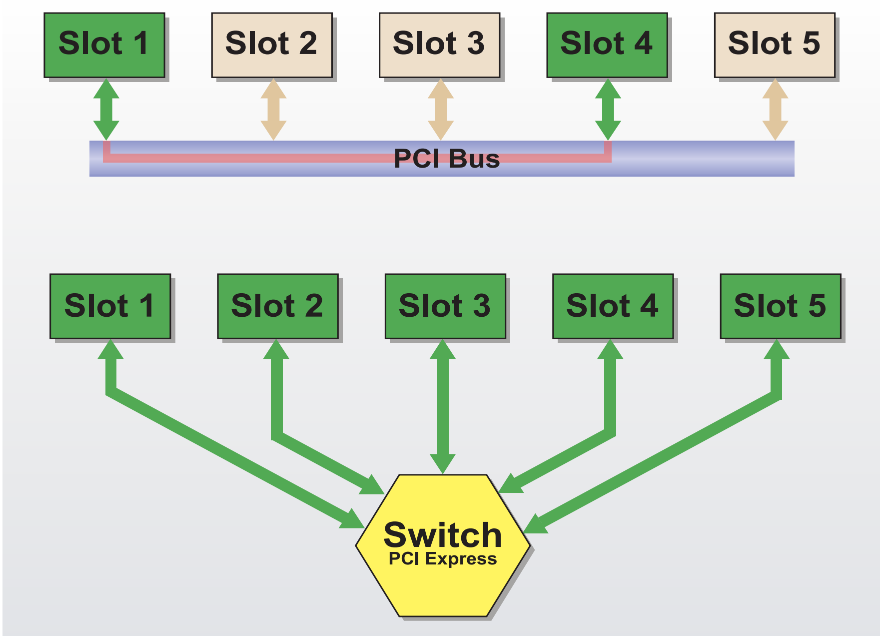

Figure 4

tages presented by the newer CompactPCI Express technology. Combining both new and old in this way is an ideal method of bridging the generation gap. The advantages of CompactPCI Express, such as cost reduction through a simple serial bus structure, high data transfer rates, and future-proof design, are combined with backward compatibility with existing CompactPCI technology. Figure 5 shows that the PCI compatible layer structure of CompactPCI Express allows it to be used with any compatible operation system.

Since the system CPU can directly control just four CompactPCI Express slots, *switchboards* are used to distribute control if more slots are required. Hence, backplanes can have slots dedicated to one or more switchboards. In a 3U CompactPCI Express environment, up to a further seven slots can be addressed using the 1x4 lanes configuration while in a 6U environment, switchboards can have 18x4 lanes or even 8x8 lanes.

The backplane configuration, that is, the number and nature of the available slots together with the channel and lane architecture, are stored in an EEPROM device. Besides this general description of the backplane, the EEPROM stores additional information on, for example, the manufacturer, date of manufacture, lot number, and serial number.

CompactPCI Express is a universal, high-performance and future-oriented bus system for the industrial marketplace. Apart from offering just high-speed serial data transfers, CompactPCI Express, with its asynchronous communication, is equipped with CRC checksum algorithms for error recognition and correction, and provides native hot plug functions – prerequisites for a universal bus. It is expected that the first operating system to truly take advantage of all these features will be Microsoft's *Longhorn*, the successor to Windows XP, in which native support for PCI Express is embedded and hot plug of peripherals are permitted without extra, and often expensive, software overhead.

Because of the widespread distribution of this technology in the desktop marketplace, the price of the individual PCI Express components is expected to be even lower than that of the currently available PCI devices. CompactPCI Express combines the very latest communication technology with the platform compatibility and stability of CompactPCI, giving developers reason enough to use it as the basis in all conceivable industrial applications.

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Website: www.inova-computers.de

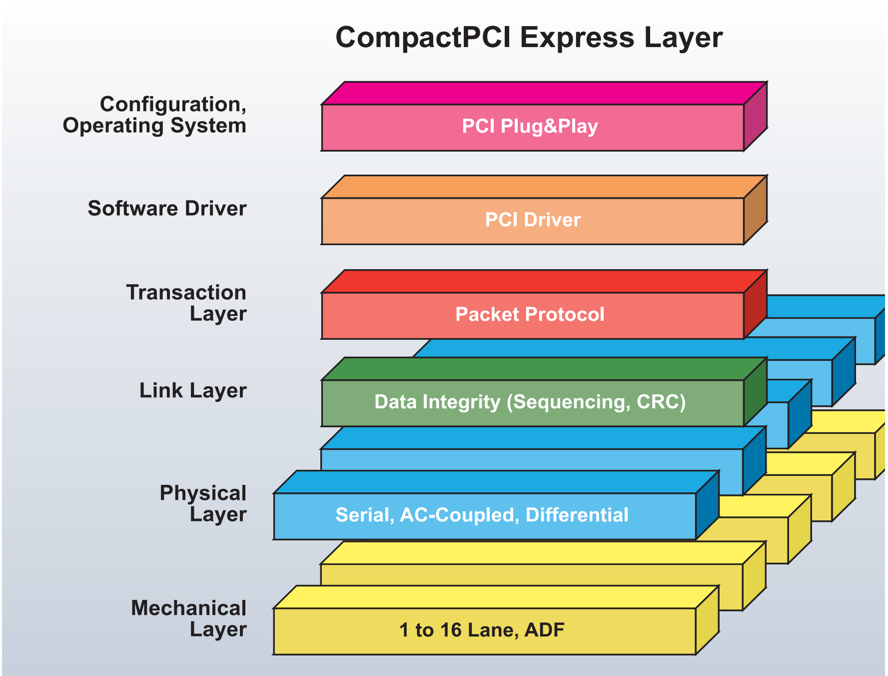

Figure 5

BUYER'S GUIDE: Processor Boards

Company Name	Celeron	Crusoe	Geode	MIPS	Multiple MPU	Pentium	Pentium II	Pentium III	Pentium 4	Pentium 4M	Pentium M	Pentium MMX	PowerPC	PowerQUICC	Socket 370	Socket 7	SPARC	x86	Xeon	Xscale	Other*	Website
Acqiris								•														www.acqiris.com
ACT/Technico														•								www.acttechnico.com
Actis													•	•								www.actis-computer.com
ADLINK Technology	•		•			•	•	•	•		•	•			•	•			•	•	2	www.adlinktech.com
Adtech															•							www.adtecheng.com
Advanet									•				•									www.advanet.co.jp/en
Advantech	•					•		•	•		•	•										www.advantech.com
Aitech Defense Systems													•									www.rugged.com
AMD																•						www.amd.com
American Portwell																			•		2	www.portwell.com
Amplicon									•													www.amplicon.co.uk
Anatel																					7	www.anatel.com
ANT Computer						•																www.antcomputer.com
Applied Data Systems																				•	8	www.applieddata.net
Arbor Technology																					3	www.arborsolution.com
																					5	
Arise							•								•							www.arisecomputer.com
Arista						•			•													www.aristaipc.com
Artesyn Communication						•							•									www.artesyncp.com
Artesyn Technologies													•									www.artesyn.com
Axiomtek											•											www.axiomtek.com
Ballard Technology													•									www.ballardtech.com
BVM																•						www.bvmltd.co.uk
Centralp Automatismes												•										www.centralp.com
CES													•									www.ces.ch
Cluster Labs						•		•														www.cluster-labs.com
Computer Modules	•							•														www.computermodules.com
Compware				•							•		•				•				2	www.compware.com
Concurrent Technologies						•		•			•								•			www.gocct.com
Continuous Computing											•						•					www.ccpu.com
Curtiss-Wright Embedded					•								•									www.cwcembedded.com
Cyclone Microsystems																					6	www.cyclone.com
Datametrics									•													www.datametrics.com
Diversified Technology										•	•								•			www.atcatogo.com
DMD Computers						•		•								•						www.dmd.it
DNA Enterprises													•									www.dna-cs.com
Dynatem						•	•	•			•				•	•			•	•		www.dynatem.com
EKF-Electronik						•		•	•		•				•							www.ekf.de
ELTEC Electronik								•					•		•							www.eltec.com
Eonic B.V.													•									www.eonic.com
esd													•									www.esd-electronics.com
EuroTecH					•		•	•								•						www.eurotech.it
Evoc Technology									•													www.evoc.com

*Other KEY: 1 Celeron M 2 Dual Pentium 3 Eden 4 ELAN 5 Ezra 6 i960 7 MPC860 8 RISC 9 Special purpose

Company Name	Celeron	Crusoe	Geode	MIPS	Multiple MPU	Pentium	Pentium II	Pentium III	Pentium 4	Pentium 4M	Pentium M	Pentium MMX	PowerPC	PowerQUICC	Socket 370	Socket 7	SPARC	x86	Xeon	Xscale	Other*	Website
Extreme Engineering													•									www.xes-inc.com
Fastwel											•											www.fastwel.com
GD California						•	•	•														www.gdca.com
GE Fanuc Automation			•				•	•			•	•	•									www.gefanuc.com/embedded
General Dynamics							•	•														www.gdcanada.com
General Micro Systems						•		•			•		•						•			www.gms4vme.com
Geotest	•					•																www.geotestinc.com
GESPAC		•						•					•									www.gespac.ch
I-BUS								•		•	•											www.ibus.com
Inova								•	•		•										1	www.inova-computers.de
Integrated Device Technology				•																		www.idt.com
Intel								•		•	•								•	•		www.intel.com
Interface Amita			•					•														www.interface-co.com
Janz Computer						•																www.janzag.de

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*Other KEY: 1 Celeron M 2 Dual Pentium 3 Eden 4 ELAN 5 Ezra 6 i960 7 MPC860 8 RISC 9 Special purpose

BUYER'S GUIDE: Processor Boards

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JK microsystems																		•				www.jkmicro.com
Kontron	•					•		•			•		•						•		1	www.kontron.com
MEN Micro									•		•		•	•								www.menmicro.com
Mercury Computer Systems				•	•						•		•				•					www.mc.com
Microbus								•														www.microbus.com
Miriac													•									www.miriac.com
Motorola								•			•		•						•			www.motorola.com/computing
MPL												•										www.mpl.ch
N.A.T.													•									www.nateurope.com
National Instruments								•														www.ni.com
NEXCOM International						•	•	•			•				•	•						www.nexcom.com
NextCom																	•					www.nextcomputing.com
Omni Device										•												www.omnidevice.com
One Stop Systems								•														www.onestopsystems.com
Orion Technologies													•									www.otisolutions.com
Performance Technologies								•					•									www.pt.com
PowerBridge Computer											•											www.powerbridge.de
Prodrive													•									www.prodrive.nl
Protech Systems	•																					www.Protech.com.tw
QuickLogic				•																		www.quicklogic.com
RadiSys Corp						•					•											www.radisys.com
Radstone Embedded Computing													•									www.radstone.com
Sanritz Automation								•														www.sanritz.co.jp
SBE													•									www.sbei.net
SBS Technologies	•					•		•			•		•									www.sbs.com
Siemens								•														www.siemens.com
SMA		•	•			•		•		•	•										4	www.SMAcomputers.com
Smart Modular Tech.				•			•						•									www.smartm.com
Soltec						•																www.solteccorp.com
Spectrum Signal Processing													•									www.spectrumsignal.com
Technoland						•		•	•													www.technoland.com
Thales													•									www.thalescomputers.com
Themis Computer																	•					www.themis.com
Toshiba																					8	www.toshiba.com/taec
Transmeta		•																				www.transmeta.com
Trenton Technology						•					•											www.trentontechnology.com
TriEMS						•	•	•													9	www.triems.com
United Electronic Industries								•														www.ueidaq.com
V Rose Microsystems								•			•											www.vrosemicrosystems.com
VMETRO													•									www.transtech-dsp.com
Voiceboard													•									www.voiceboard.com
Westek						•											•					www.westekuk.com

*Other KEY: 1 Celeron M 2 Dual Pentium 3 Eden 4 ELAN 5 Ezra 6 i960 7 MPC860 8 RISC 9 Special purpose

ADVANCEDTCA CONNECTORS

This newly developed architecture and system layout allows manufacturers of telecom equipment a new standard for designing systems. ATCA stands for ***Advanced Telecommunications Computing Architecture***.

The basic structure is utilizing a modular concept. Application of this new structured approach allows various module designs that are compatible in layout and mechanical installation.

The PICMG Group created the PICMG 3.0 Standard. This Standard specifies the mechanical details with regards to input/output, voltage, current and connection parameters. Control, backplane layout and system architecture are part of the standard.

CONEC developed unique socket press fit contacts for this series of connectors. The socket contact utilizes high reliability screw machine components combined with stamped and formed press fit zone. CONEC has developed a new family of connector products that adhere to this new Standard. Products such as plugs and sockets, high power and signal contacts, have been developed.

This new connector series ia available with press fit and through hole contact types.

PRODUCT FEATURES:
- Rugged construction
- Special variations on request
- Polarizing system
- Screwdown hardware
- Premating contacts
- Press fit contacts
- Selective loading of contact positions

COMPACTPCI CONNECTORS

Compact PCI, this new bus architecture has been developed and adapted as the new standard by many computer system manufacturers. A group of companies formed the PICMG Consortium. PCI as it is known today, stands for ***Peripheral Components Interconnect***.

Telecom, datacom, computer, medical, instrumentation and industrial control manufacturers are implementing the CompactPCI Bus structure. This standardization brings many advantages to the designer of electronic systems.

CONEC is a member of the PICMG Group and has developed the 47 positions power connector types, adhering to the specifications outlined in PICMG 2.11 R1.0. Plug and socket types with various connection and contact styles have been developed. Press fit type, through hole type and high power contacts are available. Connectors can be selectively loaded to meet specific layout configurations.

PRODUCT FEATURES:
- Premating contacts in selective positions
- Polarizing, coding, system
- Mounting screws for PCB are available
- High reliability and longevity
- Selective loading, mixed layout contact configurations

AMERICAN CONEC®

PCI INDUSTRIAL PICMG COMPUTERS

AdvancedTCA: How did we get here?

By Eelco van der Wal

This magazine is about CompactPCI and AdvancedTCA. And I am glad that I am invited to write something about this subject too. As the chairman of the independent association PICMG Europe for quite some time, I have seen the process of change here. And this process I would like to share with you, providing some insights in a changing market. Product related items will be dealt with sufficiently by others in this magazine.

AdvancedTCA stands for Advanced Telecom Computing Architecture. As such it was the third main group of specifications that PICMG dealt with. The group consists of:

1. Passive Backplane – 1.x series
2. CompactPCI – 2.x series
3. Advanced Telecom Computing Architecture, AdvancedTCA – 3.x series

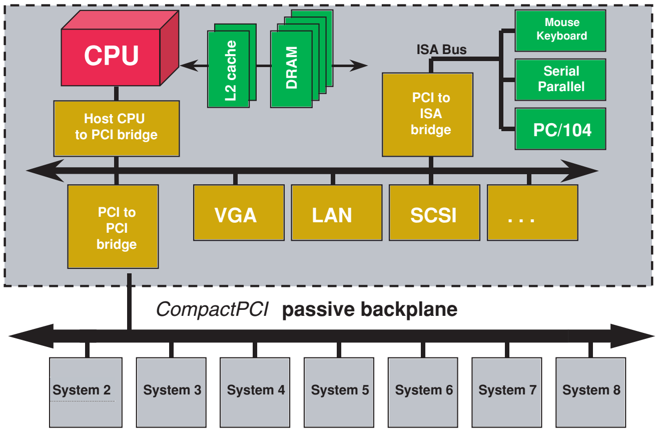

Figure 2

Historical perspective

In order to understand these different sets, a little historical overview can help. So let's go back a little in time.

The first computer bus systems became available in the 70's. These buses connected different functions, like CPU, memory, and serial interfaces for the simple reason that they did not fit on one module. The bus structure often had parallel channels for data and addresses, sometimes multiplexed together. The passive backplanes were based on this; two excellent examples are the CompactPCI and ISA bus.

If one were to build PC-like functionality at that time, it would look like Figure 1.

The system would fit on one module due to the higher level of integration of functions. As such, the computer bus, CompactPCI, becomes a system-to-system interface shown in Figure 2.

In the '70s a new serial bus, Ethernet, was defined and accepted in the office related market. Originally used to interface terminals, Ethernet was later used for what we called at the time workstations.

Now Ethernet network technology continues to be incorporated into more products than ever before. Once networked, components are relatively easy to integrate, allowing acceleration of system development. Existing network technology is naturally bridged by networked components, thus providing unparalleled system scalability. The continued ability of products to interoperate is essential to the timely development and evolution of systems in a changing world. The best example here of course is the World Wide Web, with companies like Google integrating more then 20,000 different stations. Opportunities remain for improving the rapid integration of products that will continue to adapt to the special needs of the industry.

Packet switching technology

Ethernet uses packet switching, which is based on the TCP/IP protocol. Packet switching is not new. The whole World Wide Web is based on it, connecting computers via a network. Stated differently, information spread over different systems, housing

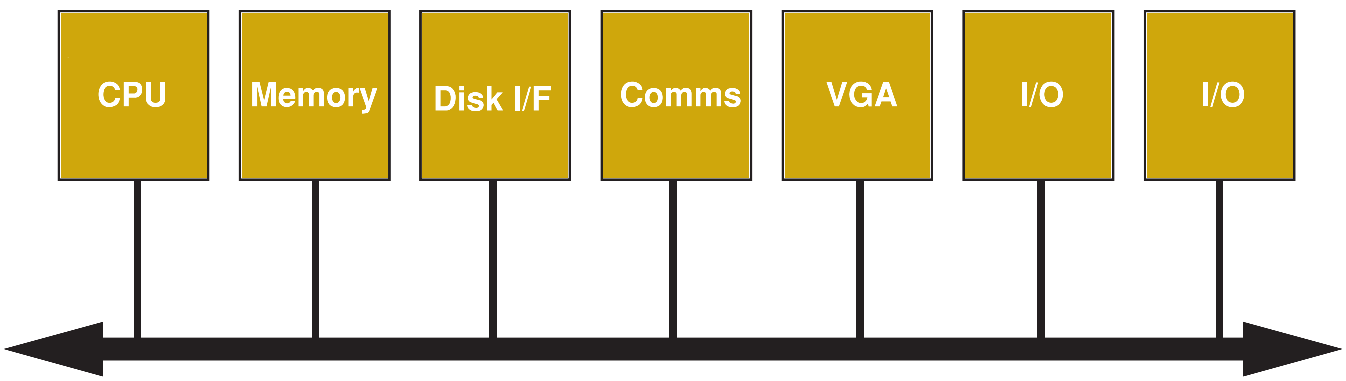

Figure 1

databases for example, are made accessible on the network onto which the system is connected using a protocol. In the case of the World Wide Web this protocol is TCP/IP.

An alternative to the parallel bus mentioned previously is packet switching backplane technology. A packet switching backplane is composed of node slots, fabric slots, and the links that interconnect them. The PSB topology can be a star (not a bus) as shown in Figure 3. Each line interconnecting a node board and fabric board represents a link that can be for example a 10/100/1000 Mbps full-duplex Ethernet connection. Node boards communicate by transferring/receiving packets to/from the fabric board, which transfers the packet to/from one or more node boards. Thus, every node board can communicate with every other node board and form a fabric.

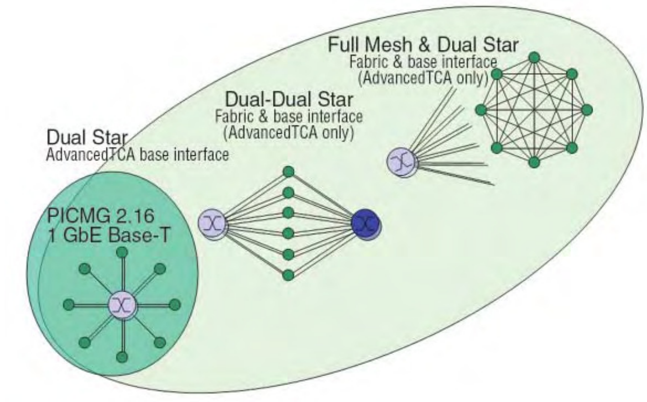

Figure 3

Basically, the idea is to incorporate the serial networking technology into a backplane. This means using it as a basis on a much smaller scale, board-to-board communication. Again this idea is not new. Technologies like MultiBus II tried to explore it ages ago. Perhaps it was just introduced too early.

The nice thing about serial buses is their hot-plug and plug-and-play behavior. One can combine both buses into one system as we do in the CompactPCI series 2.16 (based on Gigabit Ethernet), 2.17, and 2.18. These specifications support both a parallel bus as well as multiple serial buses. Networks can include:

- Ethernet
- Fibre Channel
- InfiniBand
- StarFabric
- PCI Express and Advanced Switching
- RapidIO

Working with just a serial bus, and implementing many of them in one system, brings us to the level of AdvancedTCA. The Single Board Computers (SBCs) are termed *blades*. Often blades include multiple DSP modules on a single board, or multiple CPUs.

With serial buses, several topologies can exist, connecting the intelligent modules in different ways. The crucial factor includes how the different nodes are connected: all on one line (like conventional Ethernet) via dual channels, or one-to-one. These options include star topology, dual star, and full mesh. The AdvancedTCA backplanes can support multiple versions of this.

Which bus to support?

The move to serial buses, or packet switching, comes from the need for high availability systems, with an uptime still 99.999 percent. This high level of availability begs for redundant systems. Redundant systems can more easily be built and maintained with serial buses. CompactPCI is a parallel bus. AdvancedTCA is a serial bus.

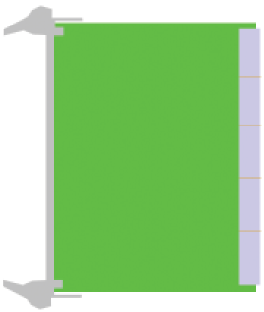

Figure 4a

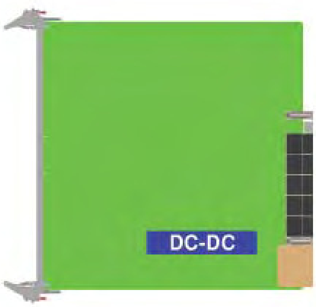

Figure 4b

	CompactPCI	AdvancedTCA
Board size	6U x 160 mm	8U x 280 mm
Distance between modules	0.8" board pitch	1.2" board pitch
Board area:	367 cm^2	903 cm^2 board area
Power consumption per module	35 – 50 W	150 – 200 W

Table 1

AdvancedTCA is targeted at a different world than CompactPCI, the core of the telecommunication world. As such, its properties are quite different than CompactPCI. Figures 4a and 4b and the specifications in Table 1 compare CompactPCI and AdvancedTCA.

With AdvancedTCA we enter a new era. Supporting multiple CPUs on one module requires power. Power generates heat, which has to be dissipated. For this reason, thermal considerations are a very important factor in the specification process.

CompactPCI 2.16 combines both a parallel and serial bus architecture. The comparison of CompactPCI, CompactPCI 2.16, and AdvancedTCA is shown in Table 2.

Advanced TCA is based on the core specification, PICMG 3.0. The core specification integrates a complete set of specifications including power distribution, mechanical elements, system management, connector zones and types, fabric topologies, thermal management guidelines, and regulatory guidelines.

The other specifications in AdvancedTCA series define the different serial communication networks, like Ethernet and Fibre

Attribute	PICMG 2.0 / CompactPCI	PICMG 2.16 / CPSB	PICMG 3.0 / AdvancedTCA
Board size	6U x 160 mm x .8"	6U x 160 mm x .8"	8U x 280 mm x 1.2"
	57 sq. in. + 2 mezzanines	57 sq in + 2 mezzanines	140 sq. in. + 4 mezzanines
Board power	35-50 W	35-50 W	150-200 W
Backplane bandwidth	~ 4 Gbps	~ 38 Gbps	~ 2.4 Tbps
Number of active boards	21	19	16
Power system	Centralized converter	Centralized converter	Distributed converters
	5, 12, 3.3 V Backplane	5, 12, 3.3 V Backplane	Dual 48 V backplane
Management	OK	OK	Advanced
I/O	Limited	OK	Extensive
Clock, update, test bus	No	No	Yes
Multivendor support	Extensive	Building	Since late 2003
Base cost of shelf	Low	Low-moderate	Moderate-high
Regulatory conformance	Vendor specific	Vendor specific	In standard
Functional density of shelf	Low	Moderate	High
Lifecycle cost per function	High	Moderate	Low
Standard GA schedule	1995	2001	2003

Table 2

Channel, InfiniBand, StarFabric, PCI Express and Advanced Switching, and RapidIO.

Additional specifications include the interface for mezzanine add on modules, CompactTCA (AdvancedTCA in a different form factor), and other small modular form factors.

Software support

With all the new features incorporated in AdvancedTCA, software support becomes a crucial factor for its success. For this reason, both PICMG and other related organizations are working on open specifications. Two of these are the System Fabric Plane (SFP) and the Service Availability Forum (SA Forum) interface specifications.

System Fabric Plane

The specifications SFP.0 and SFP.1 enable legacy protocols on PICMG 3.1 Ethernet and other transports over AdvancedTCA backplanes. By encapsulating these protocols on AdvancedTCA interconnect, they appear to be running over a direct connection.

SFP.0 is a Layer 2 or *shim* protocol specification for low overhead, high-speed generic encapsulation targeted at PICMG 3.1 Ethernet-based modular systems, but also has application for other PICMG 3.x and 2.16 fabric-based systems. SFP.0 is generic in the sense that it can be used to encapsulate all kinds of packet-

and cell-based traffic such as Time Division Multiplexed (TDM) and Asynchronous Transfer Mode (ATM) for transport between blades or chassis on a switched fabric.

SFP.1, also known as Internal TDM (I-TDM), is a companion protocol specification to SFP.0 that is optimized for TDM traffic over high-speed fabrics such as 1 and 10 Gigabit Ethernet (PICMG 3.1), Advanced Switching (PICMG 3.4), InfiniBand (PICMG 3.2), and so on. SFP.1 and SFP.0 together provide a complete encapsulation for TDM over Ethernet. This provides a functional replacement to the hardware-based H.110 and H.100 buses that existed in older telephony systems.

Service Availability Forum

The Service Availability Forum is a consortium of industry-leading communications and computing companies working together to develop and publish high availability and management software interface specifications to enable the delivery of continuously available carrier grade systems with off-the-shelf hardware platforms and middleware. The SA Forum then promotes and facilitates specification adoption by the industry. Initially, the Service Availability Forum will develop two interface specifications:

- The Service Availability Forum Application Interface (SAI-A) – a programming interface between applications and Service Availability middleware
- The Service Availability Forum Platform Interface (SAI-P) – a programming interface between the Service Availability middleware and platform components.

These specifications will be operating system, CPU, and platform agnostic, and will provide the ability to vertically integrate applications and systems without resorting to customization of the application for a particular platform. (Check www.SAForum.org for more information.)

Future parallel developments

A new generation has started with AdvancedTCA providing a major step forward toward high availability systems with very high bandwidth. However, its focus on the telecom market resulted in a large form factor, which hinders AdvancedTCA's acceptance in other markets. For this reason, a number of related developments are anticipated including:

1. Other form factors
2. Other bus systems

Other form factors

AdvancedTCA has limitations due to its size, both in area as well as width. A point of interest is the request from mostly European telecom suppliers to decrease the width of a standard module in such a way that an additional two modules fit into a 19-inch size rack. If this proposal is accepted, two sizes will compete for market share. To date, no new developments have been scheduled.

Another initiative deals with the AdvancedTCA concepts on the 6U form factor – simply named CompactTCA. This would be a logical extension to reach markets outside of telecom, but with high bandwidth and less space. Markets include radar systems and medical/image processing. With the concepts of AdvancedTCA in place, this would be a relatively easy jump – however, the

development of modules based on this to create systems would require major investments. Time will tell.

Other bus systems

AdvancedMC creates MicroTCA

AdvancedTCA created a need for mezzanines add-on modules. Advanced Mezzanine Cards, or AdvancedMCs fulfilled that need. AdvancedMCs are switch fabric based, hot swappable, and fully managed. The AdvancedMC is positioned to broaden AdvancedTCA by providing greater thermal and volume envelope add-in modularity for a variety of I/O, storage, and processor applications. The specifications were developed to meet the stringent telecom requirements for reliability, high availability, serviceability, and manageability, by accommodating system management and hot swap capability. It is expected that these characteristics will make AdvancedMC modules attractive in many other markets as well.

The AdvancedMC series of specifications follow the numbering pattern set by AdvancedTCA where AMC.0 creates the foundation for the mezzanine cards with definition of form factor, connector, power and thermal characteristics, management, clocking and base fabric. AMC.1 maps PCI Express onto the extended fabric interface. Additional specifications to support Ethernet, storage, and Serial RapidIO include AMC.2, AMC.3, and AMC.4 respectively.

While AdvancedMC was developed to be compatible with the AdvancedTCA architecture, AdvancedMC modules will be used in conjunction with other platform architectures including some unique new systems to be comprised exclusively of AdvancedMC modules. As its predecessors have shown, good mezzanine cards will be used wherever they can fit, which will encompass a very wide range of carrier form factors and applications.

Efforts are already underway to utilize AdvancedMC modules in new ways, including MicroTCA, in which AdvancedMC cards plug directly into a backplane, creating a physically small but very powerful system in 4U height and 300 mm in depth. This not only reduces size, but also cost, making it suitable for a much wider range of applications.

A wide variety of AdvancedMCs are becoming available, including processors, signal processing farms, network processors, storage, and I/O. By interconnecting a number of these AdvancedMCs into a single backplane, MicroTCA, as shown in Figure 5, will serve as an optimal platform for many different applications. All mezzanines conforming to the AdvancedMC standard must fit directly into MicroTCA without modification. MicroTCA is optimized for smaller scale, and more price sensitive applications and is therefore complementary to AdvancedTCA.

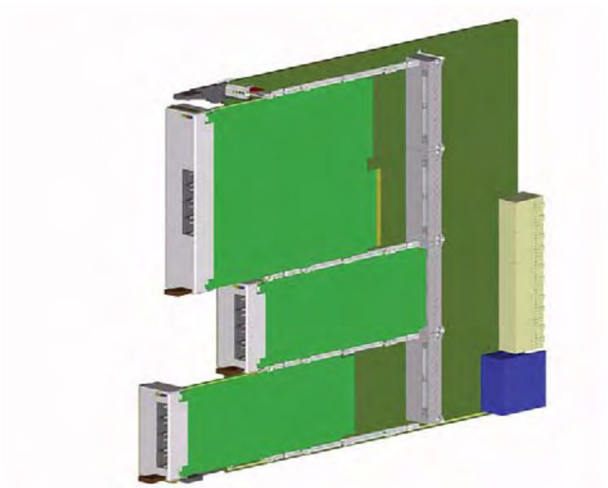

Figure 5

The application space envisioned for MicroTCA spans from sophisticated consumer electronics and business equipment on the low end to moderately complex network equipment on the high end. It includes devices to be used in telecommunications central offices, outside plant equipment like wireless basestations, and devices found in offices. Scalability at the low end is emphasized in MicroTCA, including the ability to create systems of small physical size and lower reliability levels.

Conclusion

AdvancedTCA brings a whole new level of computing architecture to the market focused on a multibillion euros industry: telecommunication. With this major achievement now becoming reality, other markets are looking to extend the high availability architectures and concepts to other form factors. With these initiatives and market drives, we will certainly see a move to packet switching and fabric planes. Depending on your future needs, it will involve you in one way or another.

***Eelco van der Waal** is chairman of PICMG Europe.*

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Industrial SBCs with an attitude

By Ernest Godsey

In the industrial automation marketplace, that old attitude of What you see is what you get *is evolving into a more pragmatic, a more adaptable approach that's making Single Board Computers (SBCs) a hot topic among system designers. Developers in the industrial sector are enthusiastic about this new breed of SBCs that come with an attitude of* What you need, I can provide.

Several suppliers have recently introduced SBCs that are better equipped than ever for industrial applications. Based on their specifications alone, these boards match up with the requirements of the industrial marketplace, but if you scratch the surface just a bit more, you'll see how targeted these SBCs can be to the specific needs of a particular application.

The best of both worlds

System designers want (and perhaps in today's marketplace they need) the best of both worlds. That is, they want solutions specific to their requirements without the added cost of a custom development. They want a standard, COTS cost-effective SBC, but they also want all of the hardware and software resources that a custom-developed, more expensive computer board would have. Not too long ago, this was an unrealistic expectation, but this new generation of CompactPCI SBCs features a level of flexibility and configurability unheard of in the past.

Recently introduced SBCs are indicative of this new generation of solutions for the industrial market segment. For example, MEN Micro's MEN F12, a 3U CompactPCI SBC based on the Freescale 5200, meets the basic requirements with capabilities including:

- Extended industrial temperature range
- Optional conformal coating to protect against chemicals, moisture, dust, and other contaminants
- Shock and vibration resistance

In addition to to these basic specifications, CompactPCI boards like the F12 have adaptable features that make their functional capabilities practically open-ended. Layered on top of the fundamental industrial specifications are flexible options that give developers a high degree of freedom in the final implementation.

Processor of-the-day

This new level of freedom even extends to the SBC's processor. The MEN F12 (Figure 1), like other solutions, is turning the old way of thinking about SBCs on its head. Not too long ago, the processor was the least changeable element on the board. Other resources, like I/O and memory, could be configured to a degree by way of mezzanine cards. But now, MEN's Embedded Systems Modules (ESM) and other vendors' System-on-Module concepts are changing the old way of thinking about SBCs.

Figure 1

Now, it's possible for the processor to be just as changeable as any other onboard resource. The F12, for example, features the PowerPC MPC5200 processor with a telematics communications unit, floating point unit, memory management unit, and DRAM controller. The processor itself is actually mounted on MEN's EM1 ESM (Figure 2) and this in turn is installed on a 3U CompactPCI ESM carrier card. If the system designer has a different set of processing requirements, another ESM featuring an entirely different processor could be installed on the 3U carrier card to provide the processing capabilities needed by the application. Or, the EM1 could just as easily be installed on a 6U or other form factor ESM carrier board compatible with practically any bus structure.

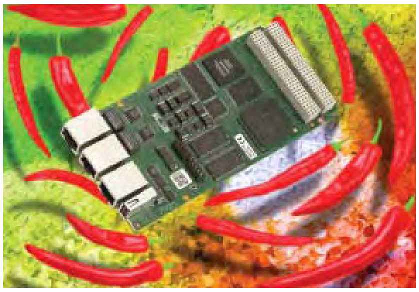

Figure 2

Of course, the I/O resources remain as adaptable as they always have been. On the F12, for example, the two onboard Fast Ethernet ports, a serial interface, and a USB channel are routed to RJ-45 connectors, but, as an alternative, they can be routed to more robust D-sub connectors. And small MEN SA-Adapters can be used to add two CAN channels to the board. Moreover, because the MPC5200 PowerPC processor features the BestComm/DMA I/O controller, other industrial interfaces such as SPI as well as CAN, USB, Fast Ethernet, and others are also supported.

Logically flexible

Another level of adaptability can be achieved with Field Programmable Gate Arrays (FPGA). The number of gates in a typical FPGA has grown to the point where multiple I/O interfaces, including the functional logic of a graphics or other type of controller, can be supported by a single programmable device. For example, an SBC with an onboard Cyclone FPGA from Altera can minimize design risks for system developers. Instead of investing significant time and effort into developing a custom PCB to provide the capabilities needed for a certain application, Intellectual Property (IP) cores can be loaded into the onboard FPGA, dramatically reducing the time and risk involved in a new development effort.

Typically, system designers utilize on-board FPGAs to implement functions such as:

- Graphics or touch-screen controllers
- I/O interfaces like CAN bus
- Digital I/O or USB ports
- Ethernet or serial channels

Some manufacturers offer a library of IP cores that can be downloaded into an FPGA. Alternatively, system designers can develop their own functional logic or acquire it from a third party.

In addition, the configuration of an FPGA need not be static, even after a particular SBC has been installed in the application. For example, the logical configuration of an FPGA can be updated dynamically while the system is running.

Open-ended options

Not so long ago, the only way that designers of industrial applications could have an SBC with the precise set of resources they needed was to design the board from scratch to meet the specifications. These days with so many options available in standard, off-the-shelf CompactPCI SBCs, in many applications a custom-designed processor card is very difficult to cost justify.

***Ernest Godsey** is president of MEN Micro, Inc., a wholly owned subsidiary of MEN Mikro Elektronik GmbH, a privately held German company. MEN supplies board-level products for embedded systems to OEMs worldwide. For the 13 years prior to his tenure with MEN, Ernest held a variety of senior management positions with Interphase Corporation in Dallas, Texas. Ernest has a BS in Electrical Engineering from Texas A&M University and a MBA from the University of Wisconsin.*

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